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24 May 1984

East Europe Report

SCIENCE & TECHNOLOGY

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EAST EUROPE REPORT

SCIENCE & TECHNOLOGY

CONTENTS

FLIGHT TESTS OF EXPERIMENTAL SHUTTLE CRAFT DESCRIBED

Warsaw TECHNIKA LOTNICZA I ASTRONAUTYCZNA in Polish No 3, Mar 84 p 13

[Article by Miroslaw Frydrych: "Flight Tests of Soviet Shuttle Craft"]

[Text] On 15 March 1983 the Soviet Union tested a shuttle craft in space. The model, called Cosmos 1445, was launched from space ship station Kapustin Jar using an SL 8 carrier rocket. This was probably the model's second flight. The previous flight took place on 3 June 1982, was designated Cosmos 1374, and occurred under similar conditions. The models were located at close orbits inclined at an angle of 50.7 degrees to the plane of the equator: 158-204 km (88.1 min) for Cosmos 1374, and 158-208 km (88.4 min) for Cosmos 1445. In both cases the trajectories of the satellites crossed the Indian Ocean at a distance of approximately 500 km from the Cocos Islands. In the area of the islands there were seven Soviet ships, including five search vessels guarded by two cruisers.

The Soviet shuttle craft is a supersonic glide aircraft and is very similar to the experimental vehicles tested in the 1970's: the German LB 21 Bumerang and the American HL 10 Lifting Body.

The weight of the model was estimated at about 900 kg, its length at about 5.5 m and its width at about 4 m.

Figure 1 [picture is not reproduced because of poor quality] shows the recovery of the Cosmos 1445 (the shuttle craft model) in the Indian Ocean. The picture shows two Soviet frogmen approaching the model floating on the waves. The model is equipped with three stabilizers, the two outer ones of which are upward-tilting wings and have control surfaces and ailerons. In the bow section we see an inflated cone intended to maintain the proper position of the model on the water and ensure the necessary stability. The cone was probably coated with a special substance making it possible to locate it more easily with radar after alighting on the water.

Figure 2 compares the American and Soviet shuttle crafts. The American shuttle craft's carrier rocket (Fig. 2a) is 57 m high (from the ground), has lift-off weight of 2,000 tons, a lift-off thrust of approximately 30,600 kN, and can lift a 29-ton load to a height of 180 km. The Soviet carrier rocket (Fig.2b) is 65 m high, has a lift-off weight of 1,500 tons, a lift-off thrust of approximately 18,000 to 27,000 kN, and can lift a 60-ton load to a height of 180 km.

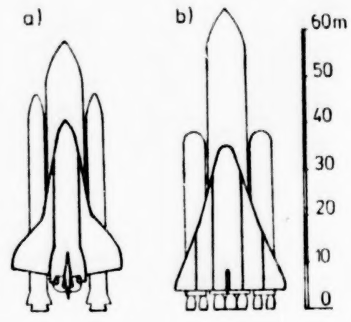

Figure 2. Comparison of American shuttle craft carrier rocket (a) with Soviet carrier rocket (b).

The shuttle craft itself is approximately 33 m long and 23 m wide. The American shuttle craft is 37 m long and 24 m wide. It is not known which type of fuel is used in the Soviet carrier rockets. Data on the Soviet shuttle craft and carrier rockets are approximate.

The choice of the Kapustin Jar space-ship station, east of Volgograd, arouses much conjecture. Up to now no tests with manned satellites have been conducted there. The recovery of the Cosmos 1374 and 1445 in the ocean is interesting, since the shuttle craft is adapted to ground landing. This may be because construction of a suitable airstrip at the Bajkonur space-ship station is not yet complete. It is also probable that the shuttle craft, in order to reduce weight, was not equipped with an undercarriage.

In 1978 test flights were conducted on a glide model shuttle craft detached from a TU-95 airplane. Resumption of tests after an interruption of several years may be explained by an attempt to match the United States in its achievements in constructing a space shuttle and the threat that possibly military activities will be carried out in space.

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TITANIUM ALLOYS, PRODUCTS, STANDARDS LISTED

Warsaw TECHNIKA LOTNICZA I ASTRONAUTYCZNA in Polish No 3, Mar 84 pp 22-23

[Article by Stanislaw Ksiazek, engineer at the Transportation Equipment Plant of the Polish Aviation Works in Mielec]

[Text] Titanium and titanium alloys are new materials which were originally used in the construction of rockets and aircraft. Their use is now being rapidly expanded to other fields of technology. The properties of titanium alloys differ from those of steel and aluminum in that the titanium alloys have high fatigue strength, particularly at high temperature and relatively low unit weight, and high corrosion resistance.

The titanium and titanium alloys used in our industry are imported from the Soviet Union, which is why the properties of these materials are shown according to Soviet standards.

The chemical compositions of the basic grades of titanium and its alloys, according to GOST 19807-14, are shown in Table 1, whereas the chemical compositions of the remaining grades used in aviation, according to Soviet standard OST 1 90013-71, are shown in Table 2.

The titanium and titanium alloys which are covered by standard GOST 19307-74 also appear in the aircraft sector standard OST 1 90013-71, which in some cases sets higher requirements (narrower spread of contents of particular components).

Forgings

The structural parts which require the greatest reliability are made from forgings. The technical requirements for forgings are given in the following standards: OST W 1 90000-70, OST 1 90002-70, TU 1-92-25-74, TU 1-92-34-75, TU 1-92--35-75, TU 1-92-36-75, TU 1-92-37-75 and AMTU 548-69.

Due to the range of the studies conducted, titanium and titanium alloy die forgings and smith forgings are divided into three groups:

--forgings which are 100 percent tested for mechanical properties and hardness,

--forgings which are random tested for mechanical properties and hardness,

Table 1. Chemical Composition of GOST 19807-14 Titanium and Titanium Alloys

(2) Gatunki tytanu lub stopów tytanu	(1) Skład chemiczny, %																	
	(3) podstawowe składniki										(4) domieszki, %							(19)
	(5) tytan	(6) aluminium	(7) mangan	(8) molibden	(9) wanad	(10) cyrkon	(11) chrom	(12) cyna	(13) krzem	(14) żelazo	(15) węgiel	(14) żelazo	(13) krzem	(10) cyrkon	(16) tlen	(17) azot	(18) wodór	suma pozostałych domieszek
WT1-00	(20) osnowa	—	—	—	—	—	—	—	—	—	0,05	0,20	0,08	—	0,10	0,04	0,008	0,10
WT1-0	,,	—	—	—	—	—	—	—	—	—	0,07	0,20	0,10	—	0,12	0,04	0,010	0,30
OT4-0	,,	0,2÷1,4	0,2÷1,3	—	—	—	—	—	—	—	0,10	0,30	0,15	0,30	0,15	0,05	0,012	0,30
OT4-1	,,	1,0÷2,5	0,7÷2,0	—	—	—	—	—	—	—	0,10	0,30	0,15	0,30	0,15	0,05	0,012	0,30
OT4	,,	3,5÷5,0	0,8÷2,0	—	—	—	—	—	—	—	0,10	0,30	0,15	0,30	0,15	0,05	0,012	0,30
WT5	,,	4,3÷6,2	—	—	—	—	—	—	—	—	0,10	0,30	0,15	0,30	0,20	0,05	0,015	0,30
WT5-1	,,	4,3÷6,0	—	—	—	—	—	2,0÷3,0	—	—	0,10	0,30	0,15	0,30	0,15	0,05	0,015	0,30
WT6S	,,	5,3÷6,8	—	—	3,5÷5,0	—	—	—	—	—	0,10	0,30	0,15	0,30	0,20	0,05	0,015	0,30
WT3-1	,,	5,5÷7,0	—	2,0÷3,0	—	—	0,8÷2,3	—	0,15÷0,40	0,2÷0,7	0,10	—	—	0,50	0,15	0,05	0,015	0,30
WT9	,,	5,8÷7,0	—	2,8÷3,8	—	0,8÷2,0	—	—	0,20÷0,35	—	0,10	0,25	—	—	0,15	0,05	0,015	0,30
WT14	,,	3,5÷6,8	—	2,5÷3,8	0,9÷1,9	—	—	—	—	—	0,10	0,30	0,15	0,30	0,15	0,05	0,015	0,30
WT16	,,	1,8÷3,8	—	4,5÷5,5	4,0÷5,5	—	—	—	—	—	0,10	0,25	0,15	0,30	0,15	0,05	0,015	0,30
WT20	,,	5,5÷7,5	—	0,5÷2,0	0,8+1,8	1,5÷2,5	—	—	—	—	0,10	0,30	0,15	—	0,15	0,05	0,015	0,30
WT22	,,	4,4÷5,9	—	4,0÷5,5	4,0÷5,5	—	0,5÷2,0	—	—	0,5÷1,5	0,10	—	0,15	0,30	0,20	0,05	0,015	0,30
PT-7M	,,	1,8÷2,5	—	—	—	2,0÷3,0	—	—	—	—	0,10	0,25	0,12	—	0,15	0,04	0,006	0,30
PT-3W	,,	3,5÷5,0	—	—	1,2÷2,5	—	—	—	—	—	0,10	0,25	0,12	0,30	0,15	0,04	0,008	0,30

Key:

1. Chemical composition
2. Grades of titanium or titanium alloys
3. Basic components
4. Dopants
5. Titanium
6. Aluminum
7. Manganese
8. Molybdenum
9. Vanadium
10. Zirconium
11. Chromium
12. Zinc
13. Silicon
14. Iron
15. Carbon
16. Oxygen
17. Nitrogen
18. Hydrogen
19. Total other dopants
20. Base

Table 2. Chemical Composition of Titanium and Titanium Alloys Covered in OST 1 90013-71 Used in Aircraft Applications

(2) Gatunek stopu	(1) Skład chemiczny, %																	
	(3) podstawowe składniki										(4) domieszki, %							(19) suma pozostałych domieszek
	(5) tytan	(6) aluminium	(7) mangan	(8) molibden	(9) wanad	(10) cyrkon	(11) chrom	(12) cyna	(13) krzem	(14) żelazo	(15) węgiel	(14) żelazo	(13) krzem	(10) cyrkon	(16) tlen	(17) azot	(18) wodór	
OT4-2	(20) osnowa	5,5÷7,0	1,0÷2,3	—	—	0,5÷2,5	—	—	—	—	0,10	0,30	0,15	—	0,15	0,05	0,012	0,10
WT4	,,	4,5÷6,0	0,8÷2,0	—	—	—	—	—	—	—	0,10	0,30	0,15	0,30	0,15	0,05	0,012	0,30
WT6	,,	5,5÷7,0	—	—	4,2÷6,0	—	—	—	—	—	0,10	0,30	0,15	—	0,20	0,05	0,015	0,30
WT8	,,	6,0÷7,3	—	2,8÷3,8	—	—	—	—	0,20÷0,40	—	0,10	0,30	—	0,50	0,15	0,05	0,015	0,30
WT18	,,	7,2÷8,2	—	0,2÷1,0	—	10,0÷12,0	—	niob 0,5÷1,5	0,05÷0,18	—	0,10	0,15	—	—	0,15	0,05	0,015	0,30

Key:

1. Chemical composition
2. Alloy designation
3. Basic components
4. Dopants
5. Titanium
6. Aluminum
7. Manganese
8. Molybdenum
9. Vanadium
10. Zirconium
11. Chromium
12. Zinc
13. Silicon
14. Iron
15. Carbon
16. Oxygen
17. Nitrogen
18. Hydrogen
19. Other dopants
20. Base

--forgings which are tested only for hardness.

The mechanical properties of die and smith forgings, 100 mm thick, determined on logitudinal specimens, are shown in Table 3.

Forging size deviations are covered in standard OST 1 41187-72.

Table 3. Mechanical Properties of Die and Smith Forgings, 100 mm Thick, Determined on Longitudinal Specimens

(1) Gatunek stopu	(2) Stan próbek badanych	(3) Właściwości mechaniczne R_m, MPa	A_5, %	Z, %	$KCU2$ J/cm²	(4) Twardość wg Brinella (średnica odcisku 10) 3000 mm
			minimum			
WT1-00 (5)	wyżarzone	294÷392	25	55	120	4,9÷5,5
WT1-0	wyżarzone	392÷539	20	50	100	4,7÷5,2
OT4-0	wyżarzone	490÷637	20	45	70	4,2÷4,8
OT4-1	wyżarzone	588÷735	15	35	45	3,8÷4,3
OT4	wyżarzone	686÷882	10	30	35	3,6÷4,2
OT4-2	wyżarzone	931÷1079	8	25	30	3,3÷3,8
WT4	wyżarzone	833÷1030	10	30	35	3,4÷3,9
WT5	wyżarzone	735÷931	10	25	30	3,4÷4,0
WT5-1	wyżarzone	784÷981	10	25	40	3,4÷3,9
WT6	wyżarzone	902÷1079	10	30	30	3,3÷3,8
WT6S	wyżarzone	833÷981	10	30	40	3,4÷3,9
WT3-1	wyżarzone	981÷1177	10	30	30	3,2÷3,7
	(6) starzone	min. 1177	6	20	20	3,0÷3,4
WT8	wyżarzone	981÷1226	9	25	30	3,2÷3,7
	starzone	min. 1177	6	20	20	3,0÷3,4
WT9	wyżarzone	1030÷1226	9	30	30	3,2÷3,7
	starzone	min. 1196	6	17	20	3,0÷3,4
WT14	wyżarzone	882÷1079	10	35	50	3,3÷3,8
WT20	wyżarzone	931÷1128	10	25	40	3,3÷3,8
WT22	(7) obrobione cieplnie	1079÷1275	8	16	25	3,1÷3,6

Key:

1. Alloy
2. Condition of specimen
3. Mechanical properties
4. Brinell hardness, (indentation diameter 10)
5. Annealed
6. Aged
7. Heat treated

Bars

Titanium and titanium alloy hot-rolled bars are produced according to standards OST 1 90173-75 and OST 1 90266-78. These bars are produced in diameters ranging from 10 to 150 mm with an outer diameter tolerance js 16, js 17.

The mechanical properties of bars and other forms are the same as the properties of forgings.

Titanium alloy cold-rolled bars are produced according to TU 1-5-242-73 in sizes ranging from 22 to 55 mm at h14 tolerance.

Titanium and titanium alloy extruded bars are produced according to OST 1 92020--72 in diameters from 15 to 100 mm at js 18 tolerance, length of bars, 5-1.5 meters [as published].

Titanium and titanium alloy forged bars are produced according to OST 1 90107-73 and TU 1-92-38-75 in sizes from 65 to 250 mm at js 19 tolerance, with length of bars 0.5-2 m.

Bars for production of connector parts by upsetting are produced according to OST 1 90201-75 and TU 1-92-3-74 in sizes from 4 to 16.2 mm at h10 tolerance.

Sheet Metal

Titanium and titanium alloy sheet metal is produced according to OST 1 90024-71, OST 1 90042-71 and TU 1-92-41-76.

Cold-rolled sheet metal is produced in thicknesses from 0.3-10.5 mm at thickness tolerance js 15, js 16, and hot-rolled sheet metal from OT4-1 alloy is produced in thicknesses from 12 to 60 mm at js 17 tolerance.

Tubing

Titanium and titanium alloy tubing can be produced according to GOST 22897-77 and OST 1 90050-72. Outer diameters are 5.8 to 130 mm and wall thicknesses are 0.5 to 9 mm.

A list of Soviet standards for titanium materials appears in Table 4.

Table 4. Soviet Standards for Titanium Materials

Standard Number	Title of Standard
GOST 9808-75	Pigment Titanium Dioxide
GOST 17746-79	Technical Requirements for Titanium Sponge
GOST 19807-74	Grades of Titanium and Titanium Alloys for Plastic Working
GOST 22897-77	Titanium Alloy Cold-Formed Seamless Tubing
OST 1 90000-70	Titanium Alloy Die and Smith Forgings
OST 1 90002-70	Titanium Alloy Blade Die Forgings
OST 1 90006-77	Titanium Alloy Bars and Semifinished Products for Blades
OST 1 90013-78	Grades of Titanium Alloys
OST 1 90024-71	OT4-1 Titanium Alloy Plates
OST 1 90027-71	Titanium Alloy Strip
OST 1 90030-71	Grades of Casting Titanium Alloys
OST 1 90042-71	Titanium Alloy Sheet Metal
OST 1 90050-72	Technical Requirements for Titanium Alloy Tubing
OST 1 90103-73	WT5-1 Titanium Alloy Welded Rings from Hot-Rolled and Pressed Sections
OST 1 90107-73	Titanium Alloy Forged Bars
OST 1 90145-74	Titanium Alloy Foil
OST 1 90173-75	Technical Requirements for Titanium Alloy Rolled Bars
OST 1 90201-75	Titanium Alloy Ground and Mechanically Sized Bars
OST 1 90266-78	Titanium Alloy Bars

[Table continued on following page]

Table 4. [Continued from preceding page]

OST 1 92020-72	Sizes and Technical Requirements for Titanium Alloy Stamped Bars
PI 1.2.051-78	Application of High-Fatigue-Strength WR-22 Titanium Alloys
TU 1-5-242-73	Titanium Rolled Bars
TU 1-92-3-74	WT16 Alloy Bars for Cold Upsetting
TU 1-92-22-74	WT22 Alloy Bars for Fasteners
TU 1-92-25-74	WT22 Alloy Precision Die Forgings
TU 1-92-30-74	Titanium Alloy Sheet Metal for Tubing
TU 1-92-34-75	WT22 Alloy Die Forgings
TU 1-92-35-75	WT22 Alloy Forgings
TU 1-92-36-75	WT22 "Conveyor-Rail" Die Forgings
TU 1-92-37-77	WT22 Die Forgings for Steel Structures
TU 1-92-38-75	WT22 Forged Bars
TU 1-92-41-76	Special Designation OT4 and OT4-1 Titanium Alloy Sheet
MRTU 14 no.19-64	Titanium Sponge
AMTU 5468-69	Titanium Alloy Disk Die Forgings
GOST 9853.0-79	General Requirements for Analysis of Titanium Sponge
GOST 9853.1-79	--Method for Determining Nitrogen
GOST 9853.2-79	--Method for Determining Iron
GOST 9853.3-79	--Method for Determining Carbon
GOST 9853.4-79	--Method for Determining Chlorine
GOST 9853.5-79	--Method for Determining Oxygen
GOST 9853.6-79	--Spectral Method for Determining Silicon, Iron and Nickel
GOST 19863.0-74	Titanium Alloys. General Requirements on Chemical Analysis
GOST 19863.1-74	--Methods for Determining Aluminum Content
GOST 19863.2-74	--Methods for Determining Vanadium
GOST 19863.3-74	--Methods for Determining Vanadium and Chromium
GOST 19863.4-74	--Methods for Determining Tungsten
GOST 19863,5-74	--Methods for Determining Iron
GOST 19863.6-74	--Methods for Determining Silicon
GOST 19863.7-74	--Methods for Determining Manganese
GOST 19863.8-74	--Methods for Determining Molybdenum
GOST 19863.9-74	--Methods for Determining Niobium
GOST 19863.10-74	--Methods for Determining Zinc
GOST 19863.11-74	--Methods for Determining Palladium
GOST 19863.12-74	--Methods for Determining Chromium
GOST 19863.13-74	--Methods for Determining Zirconium

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ASPECTS OF CSSR CMOS INTEGRATED CIRCUITS DISCUSSED

Circuit Characteristics Surveyed

Prague SDELOVACI TECHNIKA in Czech No 10, 1983 pp 365-368

[Article by Jaroslav Kruml, d.t.: "Czechoslovak CMOS Integrated Circuits"]

[Text] Because of the lack of summary or survey data on new Czechoslovak unipolar CMOS circuits, this article gives a brief survey of the technical characteristics of the main series of these circuits. CMOS integrated circuits are a large group of unipolar circuits with complementary type N and type P channels. Depending on the input polarity, one of the transistors is always closed (Fig. 1), so that when nothing is connected to the output the positive current draw is very small (in the nanoampere range per gate). When an alternating signal is applied to the input of the CMOS circuit, the current increases linearly as a function of frequency; the power consumption becomes equivalent to that of TTL logic [transistor-transistor logic] at 10 MHz (see Fig. 2). The current draw may also be increased if the leading edges of input signals rise slowly or if the free outputs of unused gates are left unconnected. The power consumption of CMOS gates begins to increase only when the state changes. After the new output state is reached, the gate holds the information without any need to increase the rest current, in contrast to other types of logic.

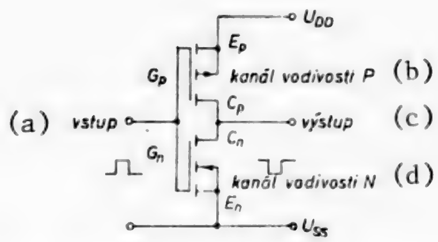


Fig. 1. Basic circuitry of complementary MOS transistors in the CMOS configuration (E = emitter; C = collector; G = gate)

Key:

a. Input	c. Output
b. P channel	d. N channel

(a)

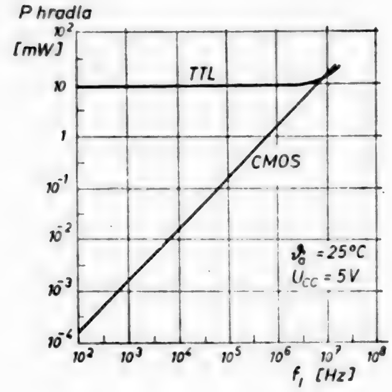


Fig. 2. Power consumption of TTL and CMOS circuits as a function of applied frequency

Key: a. Gate power consumption x 10^2 (mW)

The 4000 series unipolar CMOS integrated circuits can operate over a much wider power supply voltage range than TTL logic; U_{DD}-U_{SS} ranges from +3V to +15V. In this voltage range it is often necessary to use a stabilized power supply, which decreases device cost. Another advantage of the higher power supply voltage is the greater resistance to external interference, which increases device reliability. The unloaded output voltage (with a current draw of about 1 microampere) is almost equal to the power supply voltage. With a power volt supply voltage U_{DD}-U_{SS} = 5V, the guaranteed output voltage of a CMOS circuit is 4.9 V, while it is lower for a TTL circuit, ranging from 2.5 to 3.5 V. The output voltages of these two logic types are compared for different output voltages in Fig. 3.

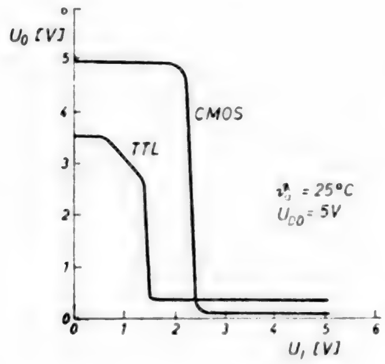


Fig. 3. Comparison of output voltages of TTL and CMOS circuits as a function of input voltage

The resistance of the closed channels is guaranteed to be less than 1,000 ohms, but it is kept well below this level in order to assure a low level of 0.4-0.8 V at 1.6 mA for TTL logic. Therefore, when CMOS and TTL circuits are connected together, an output stage such as an MHB4049 or MHB4050 must be placed between the CMOS outputs and the TTL inputs. Conversely,

when the inputs of CMOS circuits are connected to TTL outputs, the high level output voltage must be increased to at least 4 V. In many cases it suffices to connect the TTL outputs before a 3.7 kohm resistor with a power supply voltage of +5 V. An example of a transition from TTL to CMOS logic and vice versa is shown in Fig. 4.

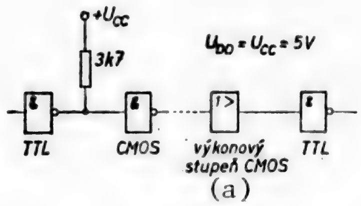


Fig. 4. Connection of TTL and CMOS circuits

Key: a. CMOS output stage

The input current I_I of CMOS circuits is extremely low compared with that of TTL circuits, typically in the nanoampere range. It is defined as the current flowing to the input relative to either U_{DD} or U_{SS} while the other inputs are connected to the opposite polarity. All inputs are protected against external electrical charges by diodes connected in the direction opposite to U_{DD} and U_{SS} (see Figs. 5 and 6).

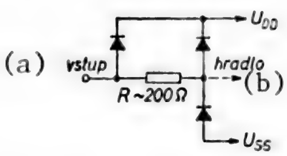


Fig. 5. Connection of protective diodes in input of CMOS circuits: earlier design

Key: a. Input
b. Gate

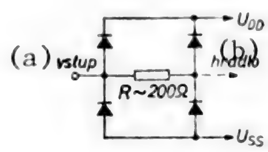


Fig. 6. Connection of protective diodes at inputs of CMOS circuits: new design

Key: a. Input
b. Gate

When designing devices with CMOS circuits the following recommendations must be observed:

--negative voltages exceeding 0.3 V must never be applied to the circuits;

--a voltage may be applied to the inputs only if the power supply voltage is connected to U_{DD}-U_{SS};

--the unused inputs must be connected (possibly through resistors) to the H or L level; otherwise the desired functioning is not guaranteed and the output may be an undefined level or the current draw I_{DD} may be excessively high.

The most-needed combinational, sequential and special circuits are currently available. They share the same limiting electrical characteristics (see Table 1) and main static parameters (see Table 2). The recommended operating conditions are given in Table 3.

Table 1. Limiting Values of Electrical Characteristics

	(a) Parametr	(b) Označení	(c) Jednotky	(d) Hodnota min.	max.
(e)	napájecí napětí	$U_{DD} - U_{SS}$	V	−0,3	18
(f)	napětí na vstupech	U_I	V	U_{SS}−0,3	U_{DD}+ 0,5
(g)	ztrátový výkon pouzdra	P_{tot}	mW		500
(h)	ztrátový výkon na jeden výstup	P	mW		100
(i)	rozsah pracovních teplot	ϑ_a	°C	0	70
(j)	vstupní proud	I	mA		±10

Storage temperature -55° to +125°C
Climatic stability categories as specified in CSN [Czechoslovak State Standard] 35 8031 0/70/21
Recommended reliability factor $\lambda = 2 \times 10^{-5}$
Resistance to soldering: 260°C, 10 sec.

Key:

a. Characteristic
b. Symbol
c. Units
d. Value
e. Power supply voltage
f. Input voltage
g. Power dissipation of package
h. Power dissipation per pin
i. Working temperature range
j. Input current (maximum current of protective diodes)

Table 2. Main Static Parameters; $\theta_a = 25°C$, $U_{SS} = 0$ V

(a) Parametr	(b) Označení	U_{DD} [V]	(c) Jednotky	(d) Hodnota min.	max.	(e) Poznámka
výstupní napětí (f) naprázdno úroveň L	U_{OL}	5 10 15	V		0,1 0,1 0,1	[1])
výstupní napětí (g) naprázdno úroveň H	U_{OH}	5 10 15	V	4,9 9,9 14,5		[2])
výstupní proud (h) úroveň L	I_{OL}	5 10 15	mA	0,5 0,8 3		U_{OL} = 0,5 V U_{OL} = 0,5 V U_{OL} = 1,5 V
výstupní proud (i) úroveň H	I_{OH}	5 10 15	mA	—0,25 —0,5 —2		U_{OH} = 4,5 V U_{OH} = 9,5 V U_{OH} = 13,5 V
vstupní napětí (j) úroveň L	U_{IL}	5 10 15	V		1 2 3	[3]) [3])
vstupní napětí (k) úroveň H	U_{IH}	5 10 15	V	4 8 12		[3])
vstupní proud (l) úroveň L	I_{IL}	5 10 15	µA		1 1 5	[2]) [4])
vstupní proud (m) úroveň H	I_{IH}	5 10 15	µA		1 1 5	[5]) [2])

1) Absolute output current 1 microampere
2) Absolute value $U_{IH} = U_{DD}$, $U_{IL} = U_{SS}$
3) Outputs held at U_{OL} = 18% U_{DD}. U_{OH} = 82% U_{DD}
4) Other inputs at U_{DD}
5) Other inputs at U_{SS}

Key:

a. Characteristic
b. Symbol
c. Units
d. Value
e. Notes
f. Output voltage, unloaded, low level
g. Output voltage, unloaded, high level
h. Output current, low level
i. Output current, high level
j. Input voltage, low level
k. Input voltage, high level
l. Input current, low level
m. Input current, high level

Table 3. Recommended Working Conditions

(a) Parametr	(b) Jednotky	(c) Hodnota	
		min.	max.
(d) napájecí napětí $U_{DD}-U_{SS}$	V	3	15
(e) napětí vstupů U_I	V	U_{SS}	U_{DD}

Notes:

1) All voltages relative to common U_{SS} or ground.
2) Negative voltages exceeding 0.3 V must not be connected to the circuit.
3) Voltage may be applied to inputs only if circuit is connected to power supply voltage $U_{DD}-U_{SS}$.
4) High or low voltage level must be applied to unused inputs.
5) CMOS integrated circuits are reinforced by soldering the pins to printed circuits or plugging into sockets. Any working position may be used.

Key:

a. Characteristic
b. Units
c. Value
d. Power supply voltage of $U_{DD}-U_{SS}$
e. Input voltage U_I

The main circuits in the CMOS series are combinational circuits, output stages and bus drivers. The series currently includes seven types of combinational circuits:

--the MHB4001 4X two-input NOR gate, $Y = \overline{A + B}$;

--the MHB4002 2X four-input NOR gate, $Y = \overline{A + B + C + D}$;

--the MHB4011 4X two-input NAND gate, $Y = \overline{A \cdot B}$;

--the MHB4012 2X four-input NAND gate, $Y = \overline{A \cdot B \cdot C \cdot D}$;

--the MHB4030 4X two-input EX-OR gate, $Y = A \cdot \overline{B} + \overline{A} \cdot B$;

--the MHB4068 eight-input NAND gate, $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$;

--the MHB4081 4X two-line AND gate, $Y = \overline{A \cdot B}$.

The circuits are packaged in plastic 14-pin DIL [dual in-line] packages. They have the recommended electrical characteristics of Tables 1, 2 and 3 and the additional electrical characteristics of Table 4. The waveforms cited in Table 4 are defined in Fig. 7.

Table 4. Supplementary Electrical Characteristics of MHB4001, MHB4002, MHB4011, MHB4012 and MHB4081 Circuits; θ_a = 25°C, U_{SS} = 0 V, C_L = 50 pF Capacitance Connected to Pin

(a) Parametr	(b) Označení	U_{DD} [V]	(c) Jednotky	(d) Hodnota min.	max.	(e) Po-známka
Klidový napájecí proud (f)	I_{DD}	5			0,5	
		10	μA		5	1)
		15			50	
zpoždění výstupního impulsu (g)		5			200	
H → L	t_{pHL}	10	ns		110	2)
L → H	t_{pLH}	15			100	
doba čela a týlu výstupního (h)		5			200	
impulsu	t_r	10	ns		100	2)
	t_f	15			80	
MHB4030						
klidový napájecí proud (f)		5			5	
	I_{DD}	10	μA		10	1)
		15			50	
zpoždění výstupního impulsu (g)		5			300	
	t_{pHL}	10	ns		200	2)
	t_{pLH}	15			150	
doba čela a týlu výstupního (h)		5			200	
impulsu	t_r	10	ns		150	2)
	t_f	15			100	
MHB4068						
klidový napájecí proud (f)		5			1	
	I_{DD}	10	μA		5	1)
		15			50	
zpoždění výstupního impulsu (g)		5			350	
	t_{pHL}	10	ns		150	2)
	t_{pLH}	15			110	
doba čela a týlu výstupního (h)		5			200	
impulsu	t_r	10	ns		100	2)
	t_f	15			80	

1) Input connected to U_{SS} or U_{DD}
2) Waveforms defined in Fig. 7a

Key:

a. Characteristic
b. Symbol
c. Units
d. Value
e. Note
f. Rest power supply current
g. Output pulse delay
h. Rise and fall time of output pulse

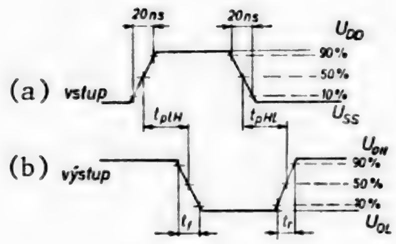
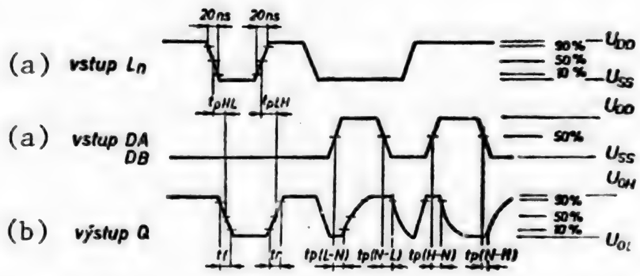


Fig. 7a. Waveform Definitions

Key:
a. Input
b. Output



N = third state (high impedance)
H = logical 1
L = logical 0

Fig. 7b. Definitions of Delay Waveforms for Transition to Third State

Key:
a. Input
b. Output

The basic series also includes the following output stages and bus drivers:

--the MHB4049 6X inverting output stage $Y = \overline{A}$;

--the MHB4050 6X noninverting output stage $Y = A$;

--the MHB4503 bus driver with tri-state output.

The MHB4049, MHB4050 and MHB4053 are packaged in 16-pin plastic DIL packages. The recommended electrical characteristics in Tables 1, 2 and 3 and the supplementary electrical parameters in Tables 5 and 6 apply to them. The wiring of the circuits and their pin assignments are shown in Fig. 8.

Table 5. Supplementary Characteristics of MHB4049 and MHB4050 Circuits; θ_a = 25°C, U_{SS} = 0 V, C_L = 50 pF Capacitance Connected to Pin

(a) Parametr	(b) Označení	U_{DD} [V]	(c) Jedn.	(d) Hodnota min.	max.	(e) Poznámka
klidový napájecí proud (f)	I_{DD}	5 10 15	µA		3 5 50	1)
zpoždění výstupního impulsu (g)	t_{pHL} t_{pLH}	5 10 15	ns		150 95 70	2)
doba čela a týlu čel výstupního impulsu (h)	t_r t_f	5 10 15	ns		140 80 50	2)
výstupní proud úroveň L (i)	I_{OL}	5 10 15	mA	2 5 15		U_{OL} = 0,5 V U_{OL} = 0,5 V U_{OL} = 1,5 V
výstupní proud úroveň H (j)	I_{OH}	5 10 15	mA	—2 —4 —6		U_{OH} = 4,5 V U_{OH} = 9,5 V U_{OH} = 13,5 V

1) Inputs connected to U_{SS} or U_{DD}
2) Waveforms defined in Fig. 7a

Key:

a. Characteristic
b. Symbol
c. Units
d. Value
e. Note
f. Rest power supply current
g. Output pulse delay
h. Rise and fall time of inp output pulse
i. Output current, L level
j. Output current, H level

Table 6. Supplementary Electrical Characteristics of MHB4503 Circuit; θ_a = 25°C, U_{SS} = 0 V, C_L = 50 pF Capacitance Connected to Pin

(a) Parametr	(b) Označení	U_{DD} [V]	(d) Jedn.	(d) Hodnota min.	max.	(e) Poznámka
klidový napájecí proud (f)	I_{DD}	5 10 15	μA		4 6 60	1)
výstupní proud úroveň L (g)	I_{OL}	5 10 15	mA	2 5 13		U_{OL} = 0,5 V U_{OL} = 0,5 V U_{OL} = 1,5 V
výstupní proud úroveň H (h)	I_{OH}	5 10 15	mA	−2 −4 −6		U_{OH} = 4,5 V U_{OH} = 9,5 V U_{OH} = 13,5 V
zpoždění výstupního impulsu (i)	t_{pHL} t_{pLH}	5 10 15	ns		100 40 30	2)
doba čela a týlu výstupního impulsu (j)	t_r t_f	5 10 15	ns		160 70 55	2)
zpoždění výstupního impulsu do třetího stavu (k)	$t_p(H-N)$ $t_p(L-N)$	5 10 15	ns		120 60 50	2)
zpoždění výstupního impulsu ze třetího stavu (l)	$t_p(N-H)$	5 10 15	ns		100 40 30	2)
zpoždění výstupního impulsu ze třetího stavu (m)	$t_p(N-L)$	5 10 15	ns		150 50 40	2)
výstupní proud v třetím stavu (n)	I_{ML} I_{MH}	5 10 15	μA		±1 ±1 ±5	

1) Inputs connected to U_{SS} or U_{DD}
2) Waveforms defined in Fig. 7b

Key:

a. Characteristic
b. Symbol
c. Units
d. Value
e. Notes
f. Rest power supply current
g. Output current, L level
h. Output current, H level
i. Output pulse delay
j. Rise and fall time of output pulse
k. Delay of output pulse to third state
l. Delay of output pulse from third state
m. Delay of output pulse from third state
n. Output current in third state

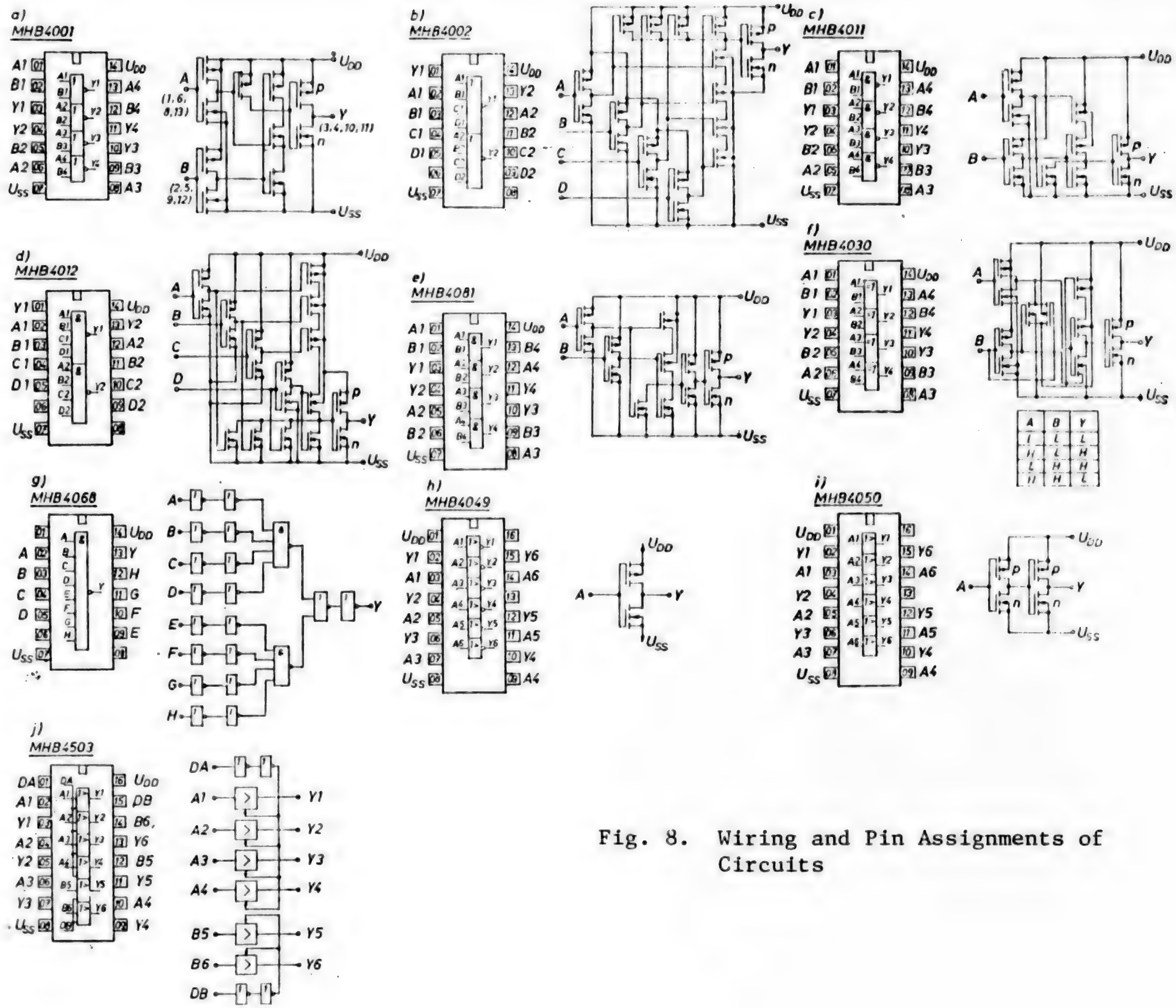


Fig. 8. Wiring and Pin Assignments of Circuits

The applications of the gates are generally known. As a supplement, Figs. 9a and 9b show two circuits in which the gates are used for a free oscillator and a crystal-controlled oscillator, since the characteristics of these components when so used differ considerably from those which are customary in oscillators using TTL gates. The free inputs can be used for blocking the oscillators. Applying a high voltage to the free input causes the oscillator to go into operation, while applying a low voltage blocks it.

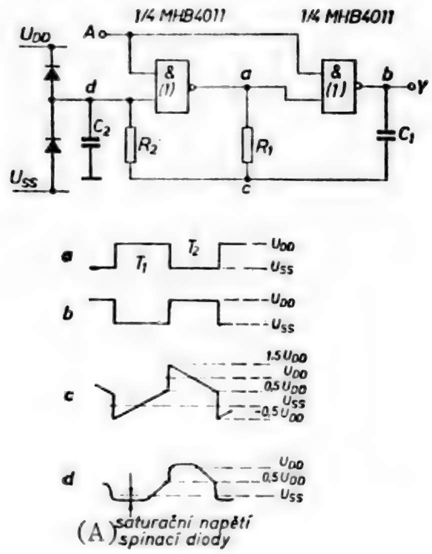


Fig. 9a. Circuit of free oscillator; waveforms at points a-b and c-d shown

Key: A. Saturation voltage of switching diode

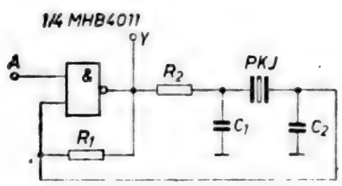


Fig. 9b. Circuit of crystal-controlled oscillator; R_1 = 1 Mohm, R_2 = 2.2 kohm, C_1 = 100 pH, C_2 = 25 pF, PKJ = 4 MHz

In the circuit of Fig. 9a the frequency of the oscillator is directly dependent on the resistance R_1 and the capacitance C_1, where $R_1 << R_2$ and $R_2 \cdot C_2 << R_1 \cdot C_1$. The output period T_p is given by the equations:

$$T_p = T_1 + T_2$$

$$T_1 = R_1 . C_1 \ln \frac{U_{DD} + U_{ST}}{U_{ST}}$$

$$T_2 = R_1 . C_1 \ln \frac{2U_{DD} - U_{ST}}{U_{DD} - U_{ST}}$$

Characteristics: R_1 = 10 kohm << $R_2 \leq$ 1 Mohm; $C_1 \geq$ 100 pf; U_{ST} = 1.2-1.7 V (threshold voltages of CMOS circuits).

The output amplitude is independent of U_{DD}, U_{ST} and temperature.

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2. Cerny, A.; Dudrova, E.; and Stehlik, V. "Zakaldny rada integrovanych obvodu CMOS [Main Series of CMOS Integrated Circuits]," collected articles from 1979 New Technology Day, TESLA VUST, Prague, 1979, p 193.

Recent Developments

Prague SDELOVACI TECHNIKA in Czech No 10, 1983 p 368

[Article: "Note on the Main Articles"]

[Text] Except for the lead article and the continuation of the series on new semiconductor components from the GDR, all of the main articles in this issue of SDELOVACI TECHNIKA deal with certain CMOS integrated circuits and some of their applications. As a result of cooperation between the ministry institute TESLA VUST [Research Institute of Communications Technology] and the TESLA Roznov and TESLA Piestany concerns, in the past 2 years CMOS integrated circuits have become available to our development organizations; we can also report the first experience with these circuits.

CMOS technology was originally designed for equipment with limited power supply capacity, and its only original advantage was its lower power consumption than all other technologies then known. But innovation has been going on in this technology, especially in the last few years, resulting in the present compatibility of CMOS with bipolar technology in small- and medium-scale integrated circuits [SSI, MSI] and with unipolar technologies in large-scale and very large-scale integration [LSI, VLSI]. Innovations in CMOS technology such as silicon gate local oxidation have reduced the shortcomings of the original aluminum gate technology (such as larger chip area requirements than unipolar forms with a single type of channel conductivity and slower operating speed than TTL). Now CMOS technologies can be used to produce even LSI circuits; the main limiting factor remains the power which the package is capable of dissipating: in plastic packages the power dissipation is about 1 W.

About 30 types of Czechoslovak-produced circuits are currently available. Most are intended for general use and are roughly equivalent to the foreign-produced circuits with the same four-digit designations, but specialized circuits for specific equipment are also produced. However, we are still in the experimental production stage, allowing an annual output of about 250,000 units, and it is not profitable to expand the number of types much beyond 30.

In terms of its use and the novelty of its application, the MHB4046 phase-lock circuit is the most interesting of the general purpose circuits (and the one on which we had the most meetings to obtain supplementary information).

The characteristics of specialized CMOS circuits are used, for example, in the MHB1115 circuit for electromechanical clocks. It contains an oscillator which oscillates at 4.1943 MHz with an external crystal resonator, a cascade of frequency dividers and a final output stage; the output of the cascade is an 0.5-Hz square wave signal. Differentiating this signal produces pulses for driving the step motor of the clock. The circuit uses a power supply of 1.2-1.7 V and draws a maximum of 80 microamperes from the oscillator.

The application of CMOS circuits, like that of all other unipolar semiconductor components, is subject to certain rules, particularly regarding the formation and discharging of electric charges. These rules and the workplace equipment involved with them must be known and kept in mind in our own work and must also be included in the directions for servicing and maintenance of our devices. The approach of "if all else fails, read the directions" will be a costly one.

In addition to the classical uses, we encounter CMOS circuits in various unaccustomed functions. Simple logic components may operate as analog circuits. SDELOVACI TECHNIKA will deal with all applications of and experience with CMOS circuits in general and Czechoslovak circuits in particular.

MHB4046 Phase-Lock Circuit

Prague SDELOVACI TECHNIKA in Czech No 10, 1983 pp 369-370

[Article by Eng Miroslav Jezek: "The MHB4046 Phase-Lock Circuit"]

[Text] The MHB4046 integrated circuit is one of a series of newly developed CMOS circuits developed by TESLA VUST. It is a phase-lock circuit equivalent to foreign circuits with the same number designation. This article describes its main characteristics and its applications, particularly in connection with a new type of phase comparator. More detailed numerical data are given in Ref. 1 and elsewhere.

The MHB4046 circuit (Fig. 1) contains a voltage-controlled oscillator (VCO), phase comparators 1 and 2, an emitter follower, a circuit for automatic creation of an offset with capacitive connection of the signal to pin 14, and an independent Zener diode with a power supply requirement of about 7 V.

The VCO

This is in essence a voltage-controlled multivibrator whose frequency is controlled by timing components R_1 and C_1 (Fig. 2). The average-frequency signal is applied to the control input 9; its voltage is half the power supply voltage. The oscillator can be tuned with good linearity, using

almost the entire power supply voltage range. The working range of the oscillator is limited by the frequency offset introduced by resistance R_2 (Fig. 3). The resistance ratio R_2/R_1 in turn determines the overall tunability of the oscillator (Fig. 4).

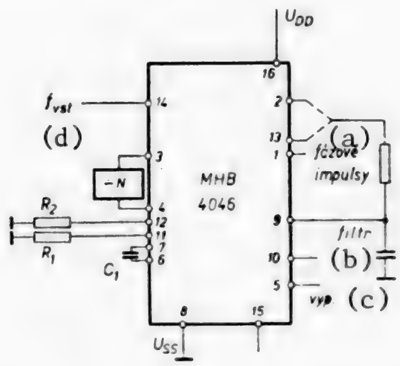

Fig. 1. Application circuit of MHB4046

Key:

a. Phase pulses
b. Filter
c. Disconnect
d. Fin

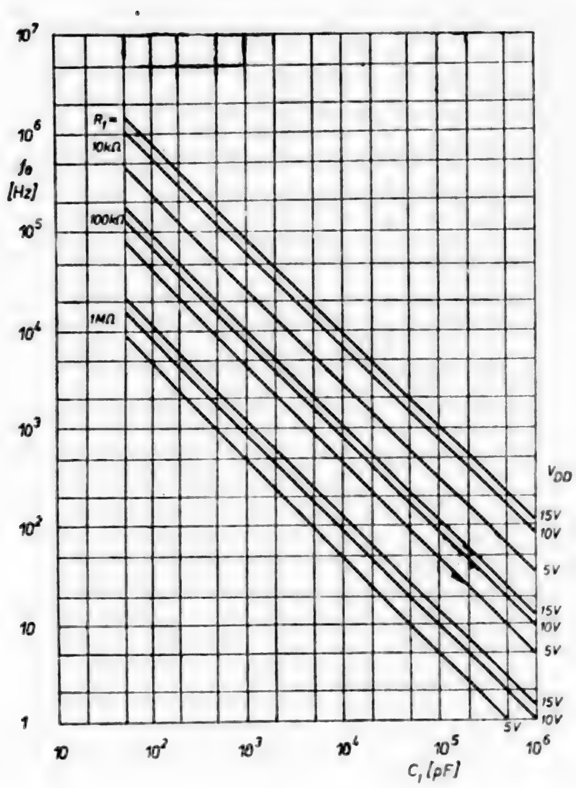

Fig. 2. Average frequency of VCO as a function of R_1 and C_1

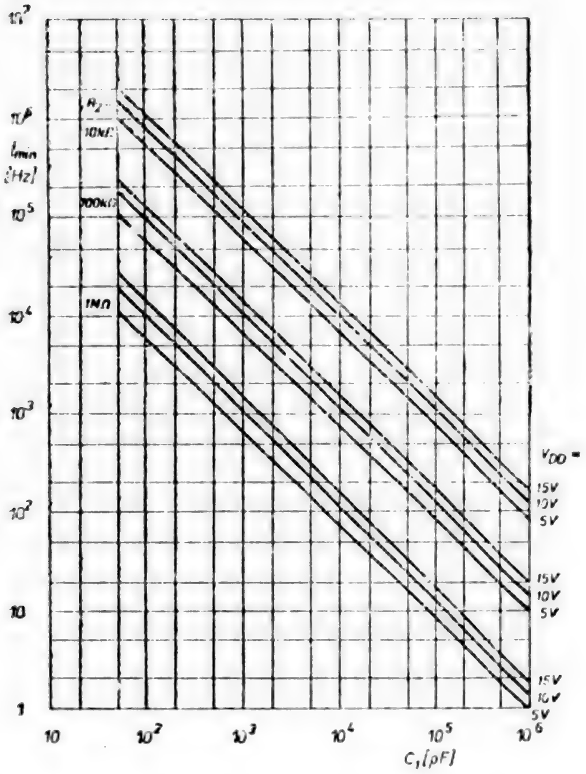

Fig. 3. Frequency offset of VCO as a function of R_2

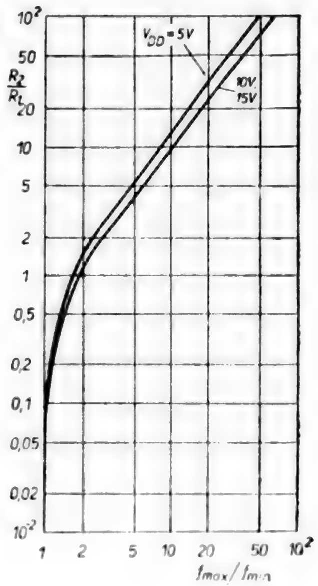

Fig. 4. Tunability of VCO as a function of R_2/R_1

The recommended range for the two resistances is 5 kohm to 1 Mohm, capacitance C > 50 pF for U_{DD} > 10 V and C > 100 pF for 5 $\leq U_{DD}$ < 10 V. The VCO signal at pin 4 has a mark-to-space ratio of approximately 1 : 1 over the entire tuning range. The oscillator control signal is fed out through the emitter follower to pin 10 for control purposes. The VCO and follower can be disconnected by applying a logical 1 to pin 5, thus minimizing power consumption by the circuit.

Comparator 1

This is an EXCLUSIVE OR circuit realizing the function $y = A\overline{B} + \overline{A}B$. The comparator waveforms are shown in Fig. 5. Fig. 6 shows the average comparator output voltage as a function of the phase difference between the signals at pins 3 and 14. This curve applies for a 1 : 1 input signal mark-to-space ratio. When the mark-to-space ratio of one of the input signals is changed, the slope of the curve and the output gain K_d of the comparator (V/rad) are changed, with all of the attendant phase-locking consequences.

In the absence of one input signal to the comparator, the average output voltage is equal to half of the power supply voltage and the frequency of the VCO is set in the middle of the working band. The comparator has considerable noise immunity. Its operating principle also gives it the ability to compare the VCO frequency with a control signal that is a harmonic. This feature can be used in several applications, but when the oscillator is tuned over a wide interval (particularly without an offset) it may jump to the control frequency.

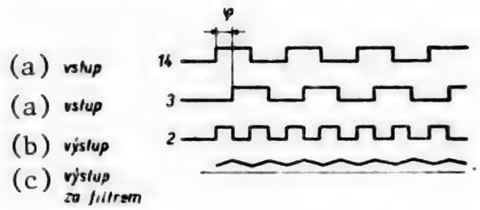

Fig. 5. Waveforms of signal from comparator 1

Key:
- a. Input
- b. Output
- c. Output after filter

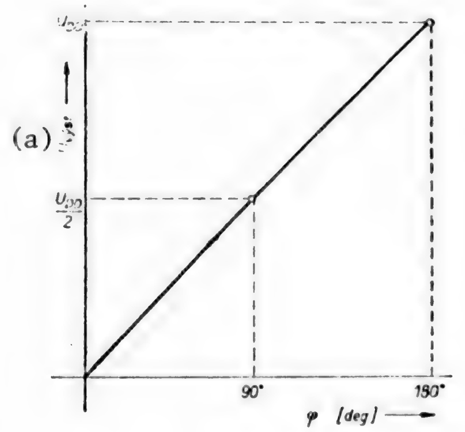

Fig. 6. Average output voltage of comparator 1 as a function of phase difference in input signals

Key: a. U_{out}

Comparator 2

The function of the second phase comparator is somewhat unusual and its particular characteristics require a somewhat different approach in design calculations for the phase-locked loop. The comparator consists of four flip-flops which react to the order of arrival of the leading edges of the two input signals. This results in a lower immunity to noise and to random disturbances, but also makes it independent of the alternation of input signals. The result of the comparison is a pulse which connects pin 13 to the power supply (U_{DD}) or zero (U_{SS}) potential.

For the rest of the time the output is disconnected (third state). One feature of this comparator is the near-zero phase difference between the output signals in the phase-locked state. The output pulses are narrow, as shown in Fig. 7, and are difficult to "see." Ideally they alternate. They are also fed to pin 1, where the actual "polarity" of the pulses at pin 13 cannot be distinguished because of the bipolarity of the pin.

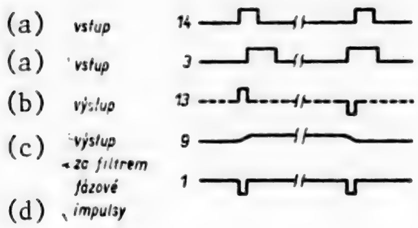

Fig. 7. Waveforms of signals from comparator 2

Key:

a. Input
b. Output
c. Output after filter
d. Phase pulses

If both input signals have the same frequency but a large phase difference, the width of the output pulses is proportional to the phase difference until phase comparison takes place. Thus the circuit operates temporarily in the so-called "injection mode." When one input signal is lacking, the comparator output has a zero control voltage and the VCO is set to the lowest frequency in the working range.

The use of the second comparator in the phase-lock circuit also insures that the holding and lock-in bands are the same and makes it independent of the filter used.

The first and second phase comparators have a common pin 14 with automatic biasing circuit. This allows capacitive connection of the input signal of different shape with an amplitude in the hundreds of millivolts (see Ref. 1).

The biasing circuit is a power-supply voltage divider consisting of two long-channel MOS transistors. The voltage from the divider, equal to half the power supply voltage, holds the first inverter at pin 14 in a linear mode. This makes the input very sensitive. A series of further inverters creates the amplified signal.

Both phase comparators can also be used in a frequency range above the maximum frequency of the VCO. They have also been tested with an external 7,200 kHz crystal oscillator (see Fig. 8).

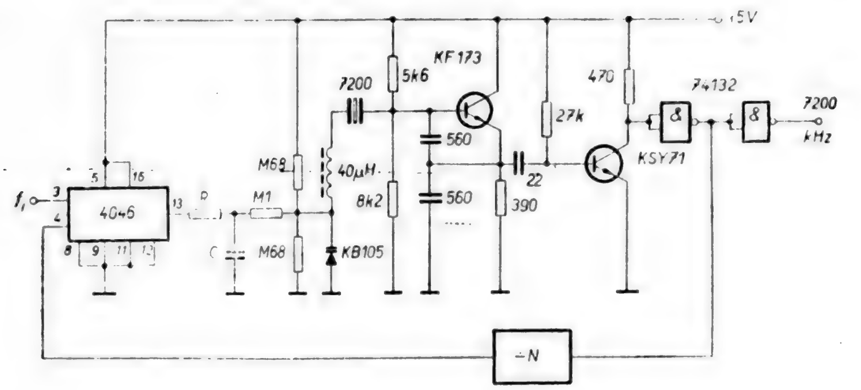

Fig. 8. Circuitry of phase lock circuit with external 7200 kHz oscillator (pin 4 should be labeled 14)

When the second comparator is used in the phase-locked loop, its output can also be used for simple indication of the synchronous state (see Fig. 9).

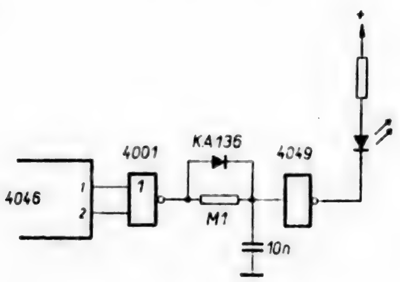

Fig. 9. Phase lock indicator circuit

As indicated by Figs. 5 and 7, in the synchronous state the logical 1 pulses at pin 2 will coincide in time with the logical 0 pulses at pin 1. The output of the 4001 gate will then be constantly at logical 0 and the light-emitting diode will not light. If there is even a brief loss of synchronization the capacitor rapidly discharges through the diode. Resistance R determines the discharge time constant and thus the length of time for which the diode is lit. If there is only a slight frequency difference when there is a loss of synchronization, the diode will flash at the beat frequency. The 4049 circuit should be used as shown in the figure only with a rather large current draw at the pin.

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Improved, Cheaper SIPMOS Circuits

Prague SDELOVACI TECHNIKA in Czech No 10, 1983 p 370

[Article: "More Favorable Prices for SIPMOS"]

[Text] MOS power transistors have already been on the market for more than 3 years. But in spite of their unquestioned superiority, they have not taken over the field below 500 V. The reason is that they cost more than bipolar transistors. Siemens has now succeeded in improving its production technology to the point that the chips for low-voltage transistors have half the surface area with the same power. This improves their electrical characteristics and decreases their price.

The new production technology has increased current density. Below 200 V, the permissible current draw is now doubled. The double ion implantation of the channel regions has remained unchanged, but the regions are shorter, so that more transistors can be placed on this chip.

The new series designated BUZ71 is intended for 50, 100, 400 and 500 V. The chips all measure 2.5 x 3.5 mm. The BUZ71 for 50 V has a resistance of 0.1 ohms in the on state, which was previously achieved on a chip with twice the area. These smaller chips also have a shorter switching time and lower capacitance.

Transistors of the BUZ71 series are installed in TO-220 plastic packages (Fig. 1). The producer expects that the price of these transistors will ultimately increase their entry into applications that have long been publicized, such as circuits for discharge tubes, switched power supplies for amusement electronics, automotive electronics, domestic appliances and machinery, computer peripherals and controllable battery chargers. The first deliveries should be made in the spring of 1983.

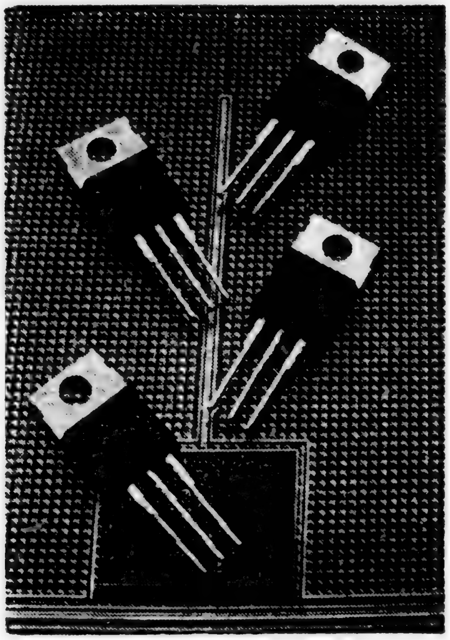

Fig. 1. SIPMOS BUZ71 transistors

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Phase-Locked Loop Design With MHB4046

Prague SDELOVACI TECHNIKA in Czech No 10, 1983 pp 371-373

[Article by Eng Pavel Hasan, CSc.: "Designing Phase-Locked Loops With the MHB4046 Integrated Circuit"]

[Text] This article discusses the design of phase-locked loops [PLL] using the CMOS integrated circuit with the type designation MHB4046, which was developed and is now being produced by TESLA VUST's experimental microelectronics organization [1, 2]. The circuit contains a phase detector which allows PLL's of remarkable characteristics to be designed. This is phase detector No 2 [3], containing a circuit which is called a "charge-pump" circuit in English. Hence arises the term "charge-pump PLL" for a PLL with this type of phase detector.

This article explains the functioning of the charge-pump PLL, presents the main equations which apply in the linear mode and describes the design method. The diverse applications of the MHB4046 are illustrated by two examples of PLL's with different properties.

Operating Principle of the Charge-Pump PLL

A block diagram of a charge-pump PLL is shown in Fig. 1, where PFD is a phase-frequency detector, CP is the charge pump circuit, LF is a filter, and VCO is a voltage-controlled oscillator [4]. The phase-frequency detector has input R for the reference signal, input V for the VCO signal, and two outputs, U and D ("up" and "down").

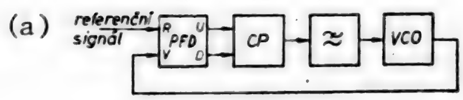

Fig. 1. Block diagram of charge-pump PLL

Key: a. Reference signal

The waveforms at the inputs and outputs of the phase-frequency detector are shown in Fig. 2. If the reference signal phase leads that of the controlled oscillator, the leading edge of the pulse at input R brings output U into the active state, which lasts until a pulse leading edge arrives at input V. Output D remains inactive. But if the VCO signal leads the reference signal, the leading edge of the pulse at input V activates output D, which stays active until a leading edge arrives at input R. In this case, output V remains inactive. Thus the phase-frequency detector has three permitted states: U (output U active), D (output D active) and N (both outputs inactive).

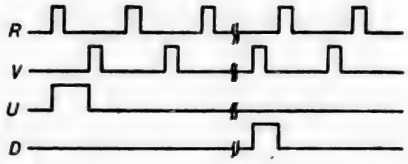

Fig. 2. Waveforms of phase-frequency detector signals

The charge-pump circuit can be modeled by two current sources and a switch controlled by the states of the phase-frequency detector (see Fig. 3). If the switch is in state U or D, the filter passes a current $\pm I_p$ with an impedance $Z_F(p)$, while in the neutral state N the phase-frequency detector is disconnected from the filter. The charge-pump circuit thus converts the three states of the PFD into the analogous values of the control voltage v_c, which, as in conventional phase detectors, adjusts the frequency of the VCO. The existence of the third (neutral) state N, however, gives the charge-pump PLL new and unique properties.

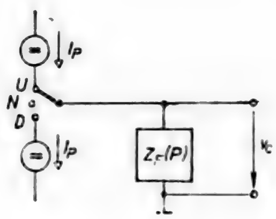

Fig. 3. Charge-pump circuit model

Linearized Model

An exact analysis of the charge-pump PLL must take account of discontinuous changes of the pump current between the values $-I_p$, 0, and $+I_p$ during each input signal cycle. But if the bandwidth of the PLL is much less than the input frequency, the state of the system changes very little during each cycle. Adequate information on the behavior of the PLL comes from a knowledge of the time behavior of the circuit parameters when averaged over a period of time much longer than the period T_i of the input signal. If we limit ourselves below to small phase errors, we can treat the charge-pump PLL as a linear system whose parameters are constant over time and can apply the methods of classical circuit theory to it.

Assume that the PLL is in the synchronous state. We designate the angular frequency of the input signal as ω_i, the phase of the input signal as Θ_i, the phase of the controlled oscillator by Θ_0 and the phase error by $\Phi = \Theta_i - \Theta_0$. The time during which one of the inputs of the PFD is in the active state is given by the equation

$$t_p = \frac{|\Phi|}{\omega_i}. \qquad (1)$$

During each input signal cycle, a pump current $\pm I_p$ passes through the filter during time t_p. The average current supplied by the PFD is therefore

$$i_d = \pm I_p \frac{t_p}{T_i} = I_p \frac{\Phi}{2\pi}. \qquad (2)$$

If we now change over from variables in the time domain to their Laplace transforms, we may add equations describing the behavior of the other functional units:

$$V_c(p) = I_d(p)\, Z_F(p) = \frac{I_p}{2\pi}\, \Phi(p)\, Z_F(p) \qquad (3)$$

and

$$\Theta_o(p) = K_o \frac{V_c(p)}{p}, \qquad (4)$$

where $V_c(p)$ is the Laplace image of the control voltage, and K_0 (rad/sec-V) is the tuning sensitivity of the controlled oscillator. From equations (3) and (4) and the equation for the phase error $\Phi = \Theta_i - \Theta_0$ we may derive the transfer function of the closed phase regulation loop [5, 6]:

$$\frac{\Theta_o(p)}{\Theta_i(p)} = H(p) = \frac{K_o I_p Z_F(p)}{2\pi p + K_o I_p Z_F(p)} \qquad (5)$$

and the transmitted phase error:

$$\frac{\Phi(p)}{\Theta_i(p)} = 1 - H(p) = \frac{2\pi p}{2\pi p + K_o I_p Z_F(p)}. \qquad (6)$$

Let us now consider the simplest filter configuration: a resistance R and a capacitance C in series. Substituting the filter impedance

$$Z_F(p) = R + \frac{1}{pC} \qquad (7)$$

into equation (5) and introducing the natural frequency ω_n of the loop and the attenuation factor ζ in accordance with the usual terminology [6], i.e.,

$$\omega_n = \sqrt{\frac{K_o I_p}{2\pi C}} \qquad (8)$$

and

$$\zeta = \frac{RC}{2} \sqrt{\frac{K_o I_p}{2\pi C}}, \qquad (9)$$

we can find the closed-loop transfer function

$$H(p) = \frac{2\zeta\omega_n p + \omega_n^2}{p^2 + 2\zeta\omega_n p + \omega_n^2} \qquad (10)$$

describing the behavior of a second-order type II regulating system [5]. Thus a charge-pump PLL with a simple passive RC element has, under these assumptions, the same properties as a continuous second-order PLL with an active filter.

We now consider the stationary response of the charge-pump PLL to an abrupt frequency change $\Delta\omega$. From equation (6), using the limit theorem, we obtain

$$\Phi_s = \lim_{t \to \infty} \Phi(t) = \frac{2\pi \Delta\omega}{K_0 I_p R_p}, \qquad (11)$$

where R_p is the resistance of a parallel combination of the bleeder resistor of the capacitor, the resistance of the printed circuit board, and the output resistance of the VCO. For the usual practical values ($R_p = 10^9$ ohms, I_p = 1 mA, $\Delta\omega/K_0$ = 5 V), equation (11) gives a stationary phase error of about $3 \cdot 10^{-5}$ rad. Achieving the same phase precision with a conventional PLL with an active filter would require an operational amplifier with a DC gain on the order of 10^5.

This method of analyzing the charge-pump PLL on the basis of time-averaged circuit parameters fails to deal with two important phenomena: degradation of system stability as a result of discontinuous operation, and abrupt changes in the VCO frequency when the outputs of the PFD change to the active state. Fig. 4 shows the relationship of the maximum size of $K\tau = 4\zeta^2$ to the quantity $\omega_i\tau = 2\zeta\omega_i/\omega_n$ [4], where

$$K = \frac{K_0 I_p R}{2\pi} \qquad (12)$$

and

$$\tau = RC \qquad (13)$$

for the stable PLL operating mode.

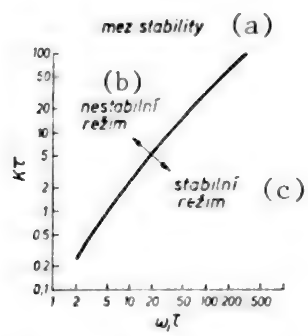

Fig. 4. Stability limit of second-order charge-pump PLL

Key:
- a. Stability limit
- b. Unstable mode
- c. Stable mode

When one of the PFD outputs changes to the active state, the control voltage v_c jumps by an amount $\Delta v_c = I_p R$. To this corresponds an abrupt change in the frequency in of the VCO:

$$\Delta\omega_0 = K_0 \Delta v_c = K_0 I_p R \, , \qquad (14)$$

producing interference components in the output signal spectrum. The undesirable jumps in the control voltage can be suppressed by adding an additional capacitor in parallel with the RC unit. But this converts the PLL into a third-order system, the study of which is beyond the scope of this article. Essentially, however, we may expect that the charge-pump PLL will not be suited to applications with stringent requirements regarding the spectral purity of the output signal (frequency synthesizers, secondary frequency references and the like).

Examples of PLL Design Using the MHB4046 Integrated Circuit

We approach the design of charge-pump PLL's as follows. We select an attenuation factor ζ between 0.5 and 2. We choose the natural loop frequency ω_n so that it is considerably lower than the input signal frequency ω_i, in line with the assumptions mentioned above. We check to see that the chosen parameters meet the conditions for stable operation (Fig. 4). From the measured tuning characteristics of the VCO we determine its tuning sensitivity K_0, and from the catalog data we find the pump current I_p. Finally, we make the filter calculations:

$$C = \frac{K_0 I_p}{2\pi\omega_n^2} \qquad (15)$$

$$R = \frac{4\pi\zeta\omega_n}{K_0 I_p}. \qquad (16)$$

This approach is illustrated by two examples of a PLL design using the MHB4046 circuit. The PLL shown in Fig. 5 is used to multiply a variable input frequency f_1 between 5 and 70 Hz by 1,000. The circuitry was designed to measure the dynamic load angle of a synchronous machine developed by the Institute for Electrical Engineering, CSAV. The natural frequency of the loop was chosen with reference to the PLL response time $\omega_n = 2\pi$ (rad/sec). The stability criterion at the lowest input signal frequency $f_i = 5$ Hz corresponds to an attentuation factor $\zeta = 0.5$. The frequency of the VCO is set by means of external resistances $R_1 = 33$ kohm, $R_2 = 1$ Mohm, and capacitance $C_1 = 330$ pF, so that a change in the control voltage v_c from 1 V to 5 V is converted into a frequency band of 5-70 kHz. From the tuning characteristics of the VCO (Fig. 6) we determine its tuning sensitivity $K_0 = 2\pi\Delta f_0/(\Delta v_c N) = 159$ rad/sec-V (Δf_0 is the shift in the frequency of the VCO corresponding to a change of Δv_c in the control voltage in the linear section of the tuning characteristic, and N is the division factor of the frequency divider in the feedback branch of the regulating loop). The producer reports a pump current $I_p = 1$ mA in phase comparator 2 of the MHB4046 circuit. Therefore equations (15) and (16) specify the values R = 248 ohms and C = 641 μF. To the circuit of Fig. 5 is added a synchronization state

indicator circuit [7]. In the absence of an input signal the light-emitting diode flashes at a frequency of 2.5 Hz. In the non-locked state it stays lit continuously, while it does not light in the synchronous state.

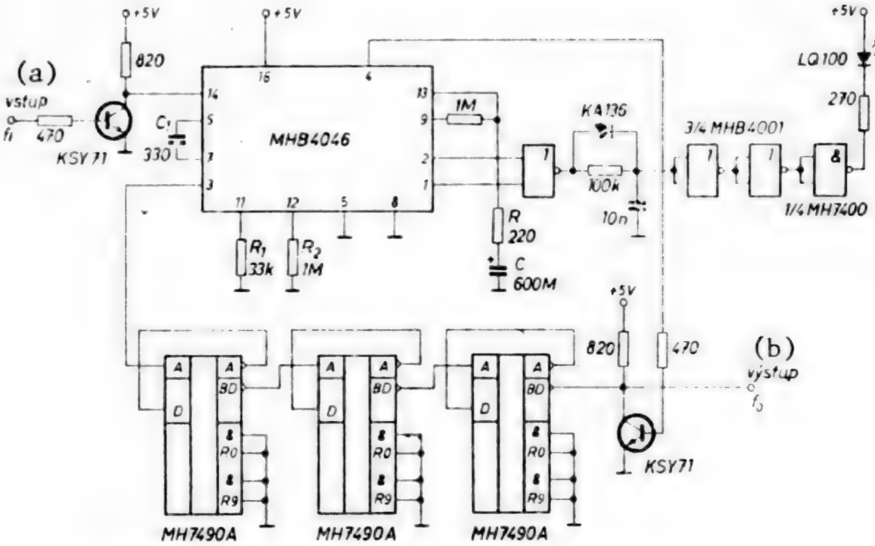

Fig. 5. Frequency multiplier for input frequency of f_i = 5-70 Hz

Key:
a. Input
b. Output

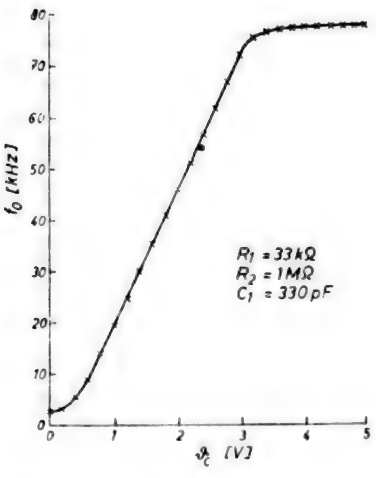

Fig. 6. Tuning characteristic of VCO of MHB4046 integrated circuit

The PLL shown in Fig. 7 uses only phase detector 2 of the MHB4046 circuit. The signal from a 6400 kHz Clapp controlled crystal oscillator is passed through a 256X frequency divider, then phase-synchronized with a reference signal X with a frequency f_i = 25 kHz, while at the same time passing through a second cascade of synchronous MH74193 downcounters, whose outputs

are set to the number K in binary code for preselection. This circuit allows a train of pulses X with a period $T_i = 1/f_i = 40$ μsec to be shifted by $(K + 1)\cdot\Delta T$, where K ranges from 0.1 to 255 and $\Delta T = 1/f_0 = 156.25$ ns. The characteristics of the charge-pump PLL allow the phase relationship between the reference signal and input pulse train to be maintained to within nanoseconds. For an attenuation factor $\zeta = 0.707$, the natural frequency of the loop is $\omega_n = 2\pi\cdot 10^2$ rad/sec and the tuning frequency of the controlled oscillator at 25 kHz, i.e., $K_0 = 8.35$ rad/sec-V, is obtained from equations (15) and (16) for a filter with R = 669 kohms and C = 3.36 nF. If narrow pulses are fed to the phase detector input, a modified circuit for indicating the synchronous state, using only output 1 of the MHB4046, has proved effective.

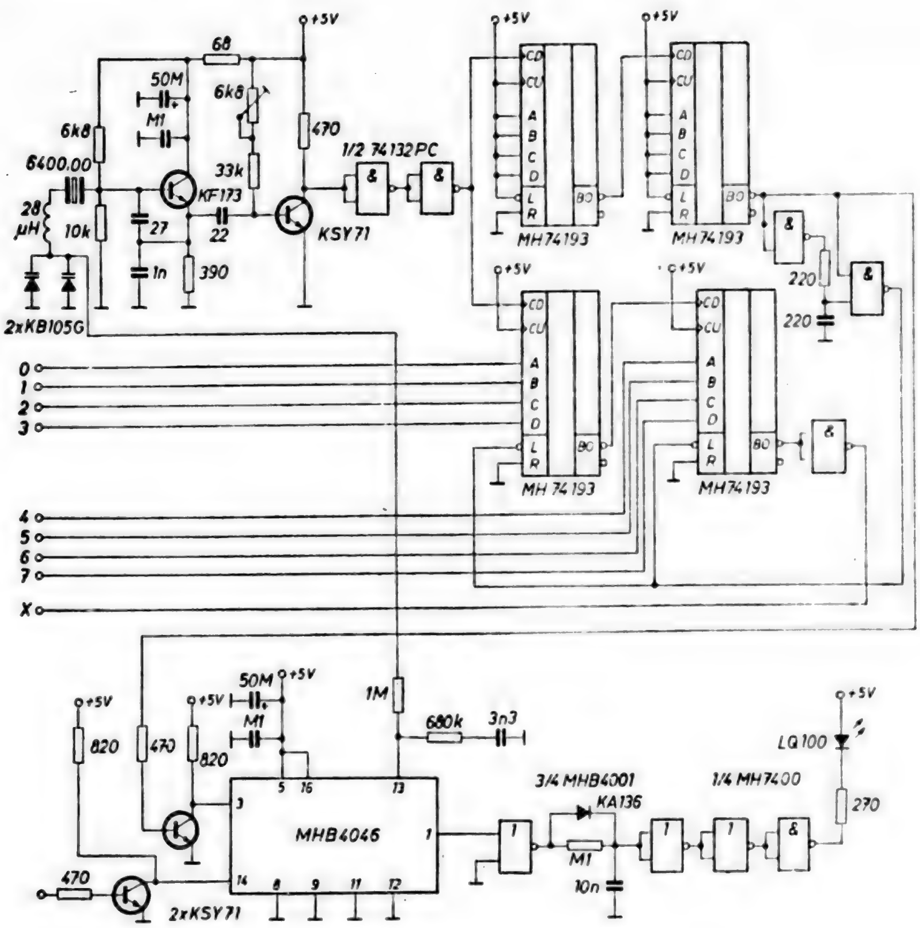

Fig. 7. Circuit for phase-shifting a train of pulses X relative to reference signal S

Conclusions

The purpose of this article has been to acquaint the reader with the characteristics and design of charge-pump PLL's, while demonstrating their advantages (extremely small stationary phase error) and shortcomings

(degradation of stability, poorer spectral qualities) and presenting examples of the design of PLL's using the MHB4046 integrated circuit.

When making a critical evaluation of the reliability of these results it must be borne in mind that the charge-pump circuit was modeled by two ideal current sources and a controlled switch for simplicity. But the outputs of phase comparator 2 of the MHB4046 are actually more similar to a voltage source. From this viewpoint, the method presented is seen as a first attempt at systematic design of a charge-pump PLL, which will give realistic results only for low values of R. Practical experience with realizations of these two systems, however, justifies the assumption that this approach is usable for approximate design of PLL's with the MHB4046 circuit if no method which gives a better indication of the actual behavior of the circuit is available.

In conclusion we may state that the MHB4046 is a welcome addition to the selection of CMOS integrated circuits produced in Czechoslovakia. It allows PLL's of noteworthy properties to be designed simply and is usable in all cases where spectral purity of the output signal is not a primary concern. Thus we may hope that it will become available to an extremely wide range of interested parties as rapidly as possible.

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Additional PLL Designs

Prague SDELOVACI TECHNIKA in Czech No 10, 1983 pp 375-378

[Article by Eng Vladimir Vachala, CSc.: "PLL's With CMOS Integrated Circuits"]

[Text] Introduction

The catalogs of several companies [1-3] and the specialized literature [4-5] make it clear that the CD4046 integrated circuit and its equivalents such as the MHB4046, the MC14046B and the HEF4046B, as well as the modernized HC/HCT4046 [7], are among the most commonly used versions. Their applications include frequency synthesis, FM demodulation, voltage-frequency conversion and the like. For higher frequencies the alternative HCTR0320 may be considered [8].

Since phase-locked loops [PLL] are used in this country, it may not be superfluous to mention their most important properties, to give useful information on the specifications of the most important auxiliary components, and to describe certain details of circuitry in order to simplify their incorporation.

Description

A phase-locked loop is a system of automatic regulating circuits consisting of a phase or frequency comparator, a low-pass filter, a controlled oscillator or multivibrator and a few other circuits, in which the regulated quantity is either phase or frequency.

The CD4046 and its equivalents have a voltage controlled multivibrator, a phase comparator and a frequency-phase comparator with common inputs, a signal follower for use in the frequency demodulator function, and an auxiliary circuit for indicating the synchronization state.

For applications where it is desirable to use a stabilized voltage source, a small Zener diode (5.2 V, 50 ohms/1 ma) is built in. Fig. 1 is a block diagram of the PLL. The parts of the 4046 are in the dotted rectangle, with the pins labeled.

PLL circuits are manufactured in CMOS technology and where possible operate with low and high values (<30% and >70%, respectively, of $U_{DD}-U_{SS}$) at which there is practically no current flow. Current is consumed during the transitions and is indirectly proportional to the number of switching operations, i.e., the frequency. Another advantageous typical characteristic is the high input impedance, about 10^{12} ohms and 50 pF. This means that the added capacitors can have a smaller capacitance and thus leads to smaller dimensions. The integrated PLL circuit may be used up to frequencies of 1.2 [1] or 1-4 MHz [2-3], or even somewhat higher [9]. The frequency limit depends on the highest attainable frequency of the multivibrator, which within certain limits can be affected by the power supply voltage (0.7 MHz at 5 V, 1.4 MHz at 10 V, 1.9-2.7 MHz at 15 V).

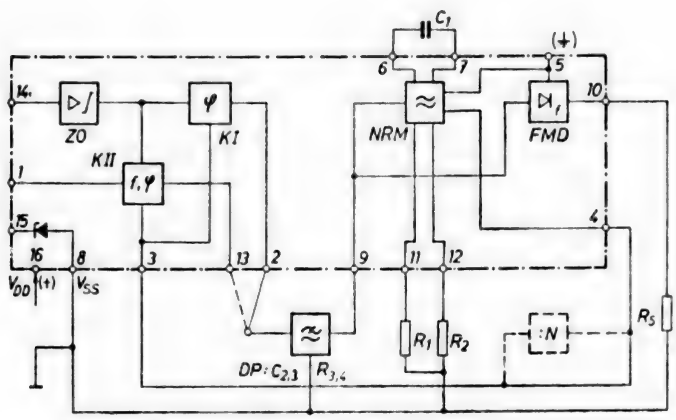

Fig. 1. Block diagram of PLL

The Voltage-Controlled Multivibrator

In Fig. 1 the voltage-controlled multivibrator is labeled NRM; Fig. 2 is a diagram of the multivibrator itself, including the associated circuit for blocking oscillation, the input circuit for the error signal, which feeds a "current mirror," and emitter follower circuits which serve as an output circuit for an FM demodulator, which is also connected to this input. The multivibrator has eight inverters and two NOR gates, forming a flip-flop circuit. The multivibrator is isolated from the load by an inverting buffer amplifier.

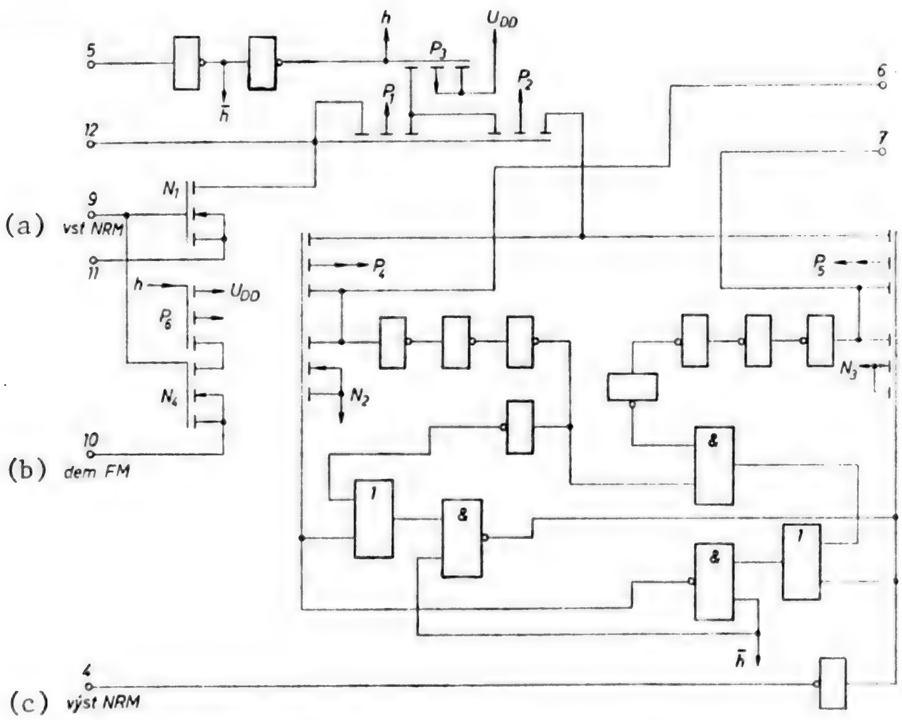

Fig. 2. Diagram of voltage-controlled multivibrator

Key:

a. Input of voltage-controlled multivibrator [NRM]
b. FM demodulator
c. Output of voltage-controlled multivibrator [NRM]

If a logical L appears at output 5 of the blocking circuit, P_3 is opened, so that P_1 and P_2 are fed the full DC voltage U_{DD} and the multivibrator can oscillate. N_1 functions as a current source, whose magnitude (with N_1 on) depends on resistance R_1. In order for the current to be linearly dependent on input voltage, R_1 must be greater than 10 kohms. The current through resistor R_1 also passes through P_1; an additional current of up to 100 percent of that passing through saturated P_3 passes through the other element (P_2) of the pair forming the "current mirror." This is used for impedance isolation of the multivibrator from the pin, but still allows it to be controlled. If resistance R_2 is less than infinity, even when the voltage at the multivibrator input (pin 9) goes to zero the current remains at the preset nonzero value (see below).

Capacitor C_1 between pins 6 and 7 is successively connected to the source of current from P_2 by means of switches consisting of pairs N_2-P_4 and N_3-P_5. The switching is controlled from the multivibrator output and begins when the voltage at C_1 reaches the threshold value which initiates toggling. Then C_1 discharges in the opposite direction and continues for the same length of time because the circuit elements are the same. The output voltage of the multivibrator is therefore a square wave with a mark-to-space ratio of 1. Its repetition frequency f_{max} is approximately given by

$$f_{max} \doteq \frac{1}{R_1(C_1+C_0)} + f_{min}, \ [\mathrm{Hz}; \Omega \mathrm{F}, \mathrm{Hz}] \tag{1}$$

when $U_{NRM\ in} = U_{DD}$ and is related to the power supply voltage by a factor of 4 [3]. Thus the calculated values must be checked on a specimen by measuring the frequency of the multivibrator when voltages U_{DD} (corresponding to f_{max}) and U_{SS} (which gives f_{min}) are applied to its input (pin 9).

The initial capacitance of the integrated circuit is C_0 = 32 pF. If $R_2 = \infty$, $f_{min} = 0$. When $R_2 < \infty$,

$$f_{min} = \frac{1}{R_2(C_1 + C_0)}, \ [\mathrm{Hz}; \Omega, \mathrm{F}, \mathrm{Hz}] \tag{2}$$

when $U_{NRM\ in} = U_{SS}$. When choosing f_{min} and f_{max}, a circuit tolerance of $\pm 20\%$ must be allowed for [3]. The temperature dependence of the frequency produced by the multivibrator is $6 \cdot 10^{-4}$ per degree C.

To determine the response of the PLL to changes in the phase or frequency of the control signal we must know the gain K of the system. This is given by

$$K = 2\pi \frac{f_{max} - f_{min}}{N}, \ [\mathrm{rad.s^{-1}}; \mathrm{Hz}, —] \tag{3}$$

where N is the division factor of the frequency divider in the feedback branch of the circuit (Fig. 1). Without the divider, N = 1. To determine the effect of resistances R_1 and R_2 on the gain, we analyze the ratio f_{max}/f_{min}: from equations (1) and (2) we have

$$\frac{f_{max}}{f_{min}} = \frac{R_2}{R_1} + 1 . \qquad (4)$$

When $R_2 \leqq R_1$, $f_{max}/f_{min} \leqq 2$, and when $R_2 \gtrless R_1$, $f_{max}/f_{min} \geqq 2$. Allowing for individual circuit tolerances [3], from equation (4), $f_{max}/f_{min} > 1.5$, i.e., $0.5\ R_1 < R_2 < \infty$. Resistors R_1 and R_2 and capacitor C_1, which determine the frequency, should be within the ranges 10 kohm $\leqq R_{1,2} \leqq$ 1 Mohm and 50 pF (for $U_{DD} > 10$ V) or 100 pF (for $U_{DD} > 5$ V) $\gtrless C_1 \leqq 0.1$ µF.

The formation of one half-period $T_0/2$ of the multivibrator is described below. Voltage u_c at capacitor C_1 reaches the threshold value u_k in accordance with the equation

$$u_k = \frac{1}{C_1} \int_0^{T_0/2} i_{c1} . dt . \qquad (5)$$

The transient charging of capacitor C_1 depends on RC_1; see also equations (1) and (2). R can be determined from the equation

$$R = \frac{u_c}{i_c} . \qquad (6)$$

The four-pole element RC_1, in the form of an integrated component (fed by an AC source) has the phase transfer function

$$\varphi = - \operatorname{arctg} 2\pi f R C_1 . \qquad (7)$$

We substitute the value of R from equation (6), where u_c is determined from equation (5); i_c = const and $f_0 = T_0^{-1}$, so that

$$\varphi = - \operatorname{arctg} \pi \frac{f}{f_0} . \qquad (8)$$

In the case of circuits determining the period or frequency of the oscillations it is useful to express the rate of change of the phase relative to frequency, $\Delta\varphi/\Delta f$. For a resonant LC circuit, it is determined from the equation

$$\left| \frac{\Delta f}{f} \right| = \frac{\Delta \varphi}{2Q} , \qquad (9)$$

where Q is the quality factor of the circuit. Using this equation, the so-called "matching quality factor" Q_S can be determined:

$$Q_S = \frac{f_0}{2} \cdot \frac{\Delta\varphi}{\Delta f} \qquad ; \quad (10)$$

From equation (8) we may determine the derivative $d\varphi/df$; changing over to finite increments, we obtain

$$\frac{\Delta\varphi}{\Delta f} = -\frac{\frac{\pi}{f_0}}{1+\left(\frac{\pi f}{f_0}\right)^2}. \qquad (11)$$

According to equation (11), when $f = f_0$, we will have $Q_S = 0.1445$ (sign omitted). Q_S is used, for example, when establishing the normalized spectral noise density [6].

The Comparators

Here weighted mixers with auxiliary analog amplifiers are generally provided, but these are not very suitable in CMOS technology [11]. Accordingly, digital comparators, designated I and II in Fig. 3, are used in the CD4046 circuit. They have a common input amplifier-limiter with four inverting stages and automatic setting of the working point.

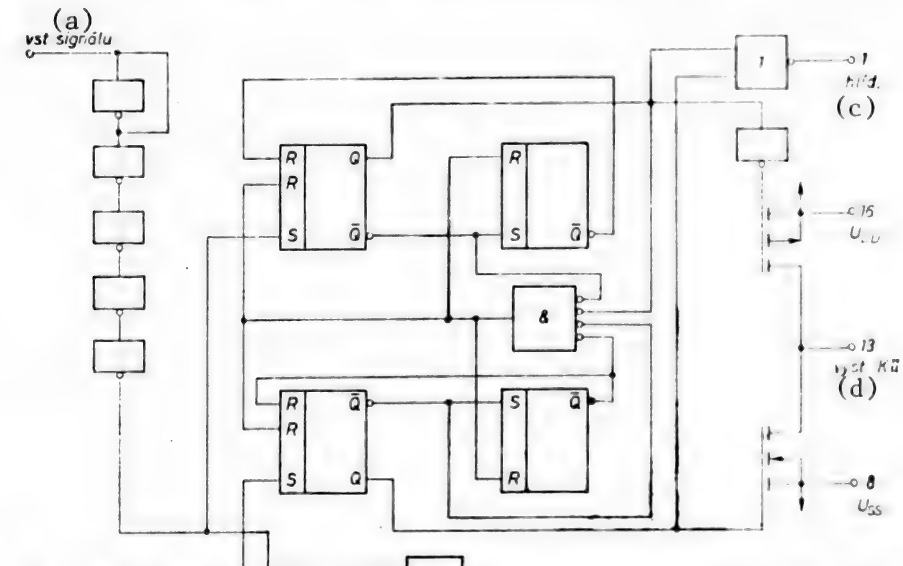

Fig. 3. Circuit with comparators I and II

Key:

- a. Signal input
- b. Comparator input
- c. Check
- d. Comparator II output
- e. Comparator I output

A digital signal can be directly applied to the input (pin 14). Signals with a small amplitude must be connected through a capacitor without a bleeder resistor. In both cases the amplifier output has a square-wave signal with constant amplitude.

The Phase Comparator (I)

This is an exclusive OR (EX-OR) circuit which operates just like a doubled overexcited weighted mixer. To avoid narrowing the lock-in band because of small amplitudes of the compared frequencies in the input waveforms, the input signal must have a mark-to-space ratio of 1. Thus the lock-in band $2f_c$ is always smaller than the stop band and is equal to

$$2f_c \doteq \frac{1}{\pi}\sqrt{\frac{2\pi(f_{max}-f_{min})}{T_1}}, \quad (12)$$

where T_1 is the time constant of simple low-pass filter R_3C_2. A further simplification can be achieved by using a proportional integrating element $R_{3,4}C_2$ (see below). The DC voltage at the output (pin 2) ranges from U_{SS} to U_{DD} for an input signal phase difference from 0° to 180°. Without a control signal, the average DC voltage $U_{DD}/2$ appears at the comparator output. The values of $R_{1,2}C_1$, are chosen so that at $U_{DD}/2$ the multivibrator oscillates at

$$f_0 = \frac{f_{max}+f_{min}}{2} \quad (13)$$

and when $R_2 = \infty$, $f_{min} = 0$.

This comparator is suitable when the input signal noise level is rather high and also when synchronizing the PLL at harmonics of the input signal. In the steady state, there is a phase difference of $90° \pm (0°$ to $90°)$ between the inputs.

The Frequency-Phase Comparator (II)

This is more complicated (see Fig. 3) and reacts only to the edges of the square wave pulses, so that it is independent of their mark-to-space ratios. The lock-in band is independent of the type of low-pass filter and is equal to

$$2f_c = f_{max} - f_{min}. \quad (14)$$

Here too, we must have $f_{min} = 0$ (and at which time $R_2 = \infty$). The comparator itself consists of four RS flip-flops, a gating circuit and a tri-state output circuit. In contrast to the previous comparator, it distinguishes whether the waveform in question has a higher or lower frequency than the synchronization signal; the output circuit (pin 13) adds to or decreases the charge on the capacitor connected to the low-pass filter until the voltage on it adjusts the multivibrator to synchrony. At this time the two transistors in the output circuit are closed, and since the input resistance

of the circuit controlling the multivibrator (pin 9) is very high, the charge from C_2 cannot flow in that direction, so that the capacitor voltage remains unchanged. It is obvious that the low-pass filter or any other circuit in this location must have no bleeder resistor. In the steady state with the comparator described, there is no phase difference between the input voltages.

The comparator is not usable when the signal only slightly exceeds the noise, or when synchronization at harmonics of the control signal is required. In the absence of a control signal the multivibrator moves to frequency f_{min}.

An auxiliary NOR circuit is attached to the comparator output to indicate the synchronization state. A high level (H) is applied to the capacitor connected to the RC low-pass filter when there is synchrony, and changes to L when they are not synchronous.

Scaling the Low-Pass Filter

In addition to components R_1, R_2 and C_1, which determine the frequency range from 0 to f_{max} or from f_{min} to f_{max}, the other external passive components of the circuit must also be specified. These include one or two resistances and an equal number of capacitors. Although like R_1, R_2 and C_1, they do not require high precision, their choice helps to determine the quality of the transient characteristics of the system, its filtering capabilities, the synchronization time, the noise properties, and, in the case of comparator I, the lock-in band.

In demanding operations, we must use control theory and establish the PLL parameters by detailed calculations. For the first design, Ref. 3 gives simple formulas:

--for a simple RC low-pass filter (integrated circuit, Fig. 4),

$$T_1 = R_3 C_2; \qquad (15)$$

--and for a proportional integrating RC element,

$$R_4 C_2 = \frac{6N}{f_{max}} - \frac{N}{2\pi(f_{max} - f_{min})} \qquad (16)$$

$$(R_3 + R_V)\,C_2 = \frac{100\,N(f_{max} - f_{min})}{f_{max}^2} - R_4 C_2, \qquad (17)$$

where R_V = 3000 ohms is the internal resistance of the integrated circuit (pin 2 or 13). The circuit of the filter is shown in Fig. 5.

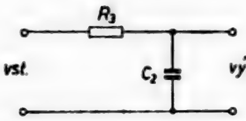

Fig. 4. Simplified low-pass filter

Key: a. Input
b. Output

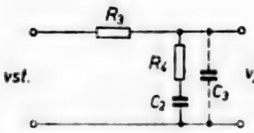

Fig. 5. Filter circuit

Key: a. Input
b. Output

Uses of PLL's

One frequent use of the PLL circuit is as an FM signal detector. The circuit is synchronized to the carrier frequency of the FM signal. The voltage at the input of the controlled multivibrator, i.e., the error voltage stripped of its high-frequency components, is demodulated by a low frequency, which also appears at pin 10. In this case the load resistance R_5 must be greater than 10 kohms [1]. The quality of the demodulator is judged in terms of the linearity of voltage detuning of the multivibrator, which is 1 percent. The graphs presented in Ref. 9 show that to obtain the most linear characteristic, C_1 must have the lowest possible capacitance. Circuitry for FM demodulation is shown in Fig. 1 [11]. The FM signal is applied to pin 14; it has an amplitude of about 0.5 V and accordingly a coupling capacitor is provided. The input resistance is about 400 kohm.

Phase comparator I is used, since the PLL must have an average frequency equal to the FM carrier signal, and also because of its good characteristics in processing signals with high noise levels. Thus $R_2 = \infty$ and the average frequency, equal to the carrier frequency, is set at 10 kHz at U_{DD} = 5 V. Then C_1 = 500 pF and R_1 = 100 kohm. According to equation (12), the lock-in band was set at $f_c = \pm 0.4$ kHz. In Figs. 1 and 4, R_3 = 100 kohm and C_2 = 1.0 μF are used to give this lock-in band. With a power supply of 5 V the demodulator consumes 132 or 92 μA for input signals with signal-to-noise ratios of 6 or 10 dB respectively. With an increasing signal level the current drain drops, because the input amplifier now works in the over-excitation region. The demodulation gain is 250 mV/kHz.

Frequency synthesis is another typical amplication of PLL's; they are most often used as selective frequency multipliers. In this case a frequency divider must be included in the feedback loop. This circuit can multiply

the input frequency by more than 1000 in a single stage, which is otherwise unattainable. Frequency-phase comparator II is used, because synchronization at some harmonic of the input frequency is not required, and the input waveform from the frequency divider generally has a mark-to-space ratio much less than 1. Because of the faster but somewhat overoscillatory transient response, and in order to obtain a smaller noise bandwidth, a proportional integrating component $R_{3,4}C_2$ is used instead of a simple RC filter.

The 4046 circuit serves very well in the low-frequency range (below 1.2 MHz) and the required ratio of undesired signal components (harmonics of the input signal, but also noise) is about 60 dB. In more demanding applications, the signal-to-noise ratio can be improved by 20 log P, in which case the multivibrator operates at the highest possible frequency and a frequency divider is added after the PLL [4, 5] (see Fig. 6). Experience indicates that crosstalk in the integrated circuits leads to transmission of undesirable spectral components to the output, which may be limited by dividing the functions over two integrated circuits, one of which operates only as a comparator, while the other functions as controlled frequency source.

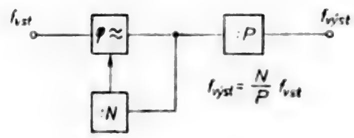

Fig. 6. Frequency divider for PLL

[f_{vst} = f_{out}; f_{vyst} = f_{in}]

Sample Realization

Input frequency f_{in} = 16 kHz, output frequency f_{out} = 208 kHz (from 192 to 236 kHz by 4-kHz increments), multivibrator frequency f_M = 832 kHz, i.e., T = 4, N = 52 (or 48-59). Circuit components: R_3 = 100 kohm, R_4 = 6800 ohm, C_2 = 1.5 μF, C_3 = 0.1 μF. U_{DD} = 12 V. Ratios shown in Table 1. In the vicinity of frequency f_{out} a selective level meter found a broad noise band of 3.1 kHz after filtering the desired frequency with a crystal bandstop filter; the measured ratio was 50 dB.

Table 1. Level Ratios

f_{vyst} [kHz]	(a)	16	160	176	192	208	224	240	256
odstup [dB]	(b)	110	92	88	86	0	85	88	98

Key:
- a. f_{out} [kHz]
- b. Ratio [dB]

A More Demanding PLL Application

In more demanding applications and at higher frequencies the controlled multivibrator is not satisfactory (because of noise and f_T). A crystal-controlled oscillator is suitable for finding fixed frequencies; but it is not a component of the integrated circuit. Its control input must have a high impedance. A circuit example [10] is given in Fig. 7.

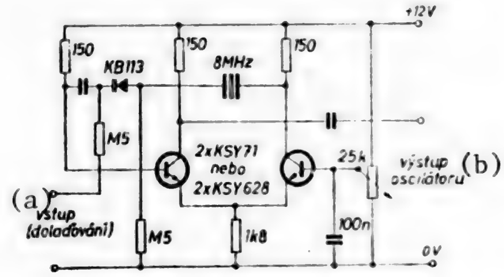

Fig. 7. Circuit of crystal-controlled oscillator

Key: a. Input (tuning)
b. Oscillator output

For this case (or with an LC oscillator), the HCTR0320 CMOS circuit, containing a programmable divider with $3 \leq N \leq 1023$ and a frequency-phase comparator with properties similar to those described above, but usable to 10 MHz [8], has recently been proposed. A block diagram is given in Fig. 8. It has a programmable divider controlled by an adder and decoder, and a frequency-phase comparator, also with a tri-state output.

The adder-decoder unit has 12 BCD [binary-coded decimal] inputs and 7 binary inputs. Here the three places of the number in BCD are added to the 7 bits of the binary number so that the sum is equal to the desired division factor N. Each decade of the BCD input is limited to a BCD number from 0 to 9. The unit operates with positive logic. All unused pins must be grounded. In some applications the emitted and received frequencies are different. It is advisable to choose the channel by means of the BCD inputs and to have the offset between the emitted and received frequencies be controlled at the binary inputs, or to use the reverse arrangement.

The selectable frequency divider is a downcounter whose cycle is repeated after N steps. The output waveform of the divider has a repetition frequency of 1/N times the input frequency, with a mark-to-space ratio of 1 : N. For fast-rising waveforms, the divider input is the only one compatible with TTL (pin 15). For slow signals or slower-rising waveforms, a Schmitt trigger is provided at pin 16. The unused input must be connected to the positive pole of power supply U_{DD}. The lowest acceptable input voltage is 5 V.

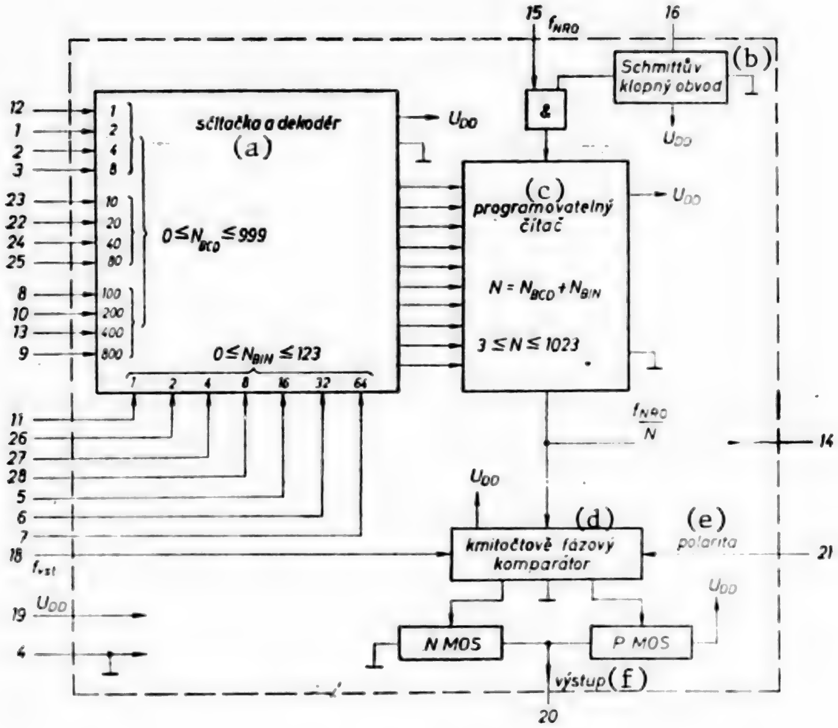

Fig. 8. Block diagram of HCTR0320 circuit

Key:

a.	Adder and decoder	d.	Frequency-phase comparator
b.	Schmitt trigger	e.	Polarity
c.	Programmable counter	f.	Output

The frequency-phase comparator compares frequencies f_{NRO} [of voltage-controlled oscillator] (pin 18) and f_{in}/N (pin 14) and emits an error signal (pin 20). The voltage there must rise from the state in which both switches at the comparator input (NMOS and PMOS) are off to the level U_{DD} or decrease to 0, depending on which of the leading edges of the signals to be compared arrives first (Fig. 9). The width of the correction pulse is proportional to the time difference, because the leading edge switches the output to the "floating" state.

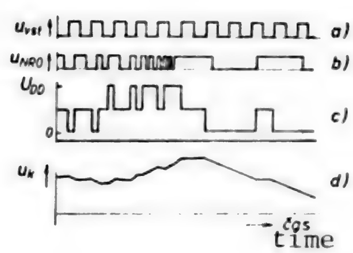

Fig. 9. Waveforms in frequency-phase comparator: a) input waveform of f_{in}; b) waveform at NRO [VCO] output with frequency f_{NRO}; c) error signal (pin 21 connected to U_{DD}); d) error signal after filtering (frequency f_{NRO} falls during rising sections and vice versa)

In choosing polarity, pin 21 must be connected to U_{DD} if the voltage of the error signal is to fall when there is an increase in the frequency of the controlled oscillator. A block diagram is shown in Fig. 10.

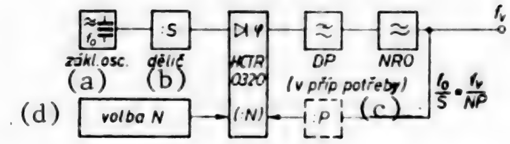

Fig. 10. Diagram of synthesizer

Key:

a. Main oscillator
b. Divider
c. If necessary
d. Choice of N

Conclusions

This article presents the characteristics of the most widely used CMOS PLL integrated circuits, describes typical uses and provides useful data for their utilization. The circuits have very low power consumption and can be used for PLL's up to 1.4 or 10 MHz.

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HUNGARIAN COMPUTER INDUSTRY SEEKS FRENCH PARTNERS

Paris ZERO UN INFORMATIQUE HEBDO in French 20 Feb 84 pp 42-43

[Article by Cecile Ixelles: "The Hungarian Computer Industry Seeks French Partners"]

[Text] For the first time, Hungary will be taking part this week in the Fifth Computer Industry Exhibit in Grenoble. The participation of the Hungarians (six companies exhibiting at one stand under the name CITH [Information Center for Hungarian Technology]) in a French show demonstrates the desire of Hungarian businessmen to export their products.

There are about 80 companies in Hungary that work in the field of computers and data processing. Exports of Hungarian computer products are made through the foreign trade firms; Metrimpex, Interog and Videoton are the largest such data processing firms in Hungary.

Cooperation between Hungary and France has existed for a long time; one example is the cooperation contract concluded by Bull-Sems (in the time of CII) and Videoton to produce data processing systems--a contract of great importance at the end of the sixties. The bonds between these two partners have grown stronger because a new Sems license contract was concluded in 1983 for 5 years.

Sztaki's Plans

To encourage technical-scientific cooperation, the two countries have CITH in Paris and the French Scientific and Technical Documentation Center in Budapest.

As Istvan Nadory, deputy managing director of the Secretariat for International Economic Relations, emphasized, "There are no such twin institutions in Hungary's relations with any other industrialized Western country."

Hungary is definitely an intellectually rich country.

To realize this all you have to do is to go into a few Hungarian research and development institutes. These national establishments, where the software is designed, are quite large.

For example, the Sztaki Institute, which was founded in 1972 and which is the data processing and automation institute of the Hungarian Academy of Sciences, has some 800 employees, of which "400 are highly qualified scientists," according to Istvan Eszes, managing director of the institute.

The Sztaki Institute has seven departments: theoretical mathematics, automation, process management, automation of the engineering industry, computer networks, electronics and CAD [computer-assisted design].

In 1970 the Institute made its first graphics terminal, the GD 70, linked to a Hungarian TAP 70/25 computer.

The next generation was the GD 80, of modular design and having a wide range of products. Its terminal was a graphics station that operated on a self-contained computer.

Today the major line of work involves the development of UNIX on the PDP11 and the 16-bit Zilog microcomputer.

The new product displayed this week in Grenoble is a graphics system, the GKS (Graphic Kanel System). It is used in Hungary to manage the movement of airlines.

The Sztaki Institute has also designed graphics modeling and movement simulation systems, designed for applications in engineering.

The Modbuil software package describes the structure of three-dimensional objects and displays the objects as thereby defined and eliminates the hidden lines. "Animator" simulates and displays the movements of these objects.

Written for the R10 computer, a version of the Mitra 15 built in Hungary under license, this software can be adapted for use on the Mitra 125 and PDP11.

The Lessons of Szamok

The Szamok Institute, a data processing training center which is at the Grenoble exhibit and which was founded 14 years ago, trains about 3,000 students per year, including 300 adults interested in entering this field.

Continuing education courses are also offered, especially in the field of micro-processing, for example in programming methodology, telecommunications, distributed computer networks, databases, computer system reliability, etc. About 30 courses are designed for foreigners.

Szamok trains specialists in all areas: analysts, programmers, operators, technicians, etc. For 2 years Szamok has also had a commercial firm, Szamalk.

This firm has 1,200 employees, about 800 of whom have a diploma from an institution of higher learning or a university, and 200 of whom have had additional studies in the United States or Western Europe according to Gyorgy Zak, director of marketing.

The staff is very well educated, but they also have another important quality: they are proficient in several languages, which makes negotiations with foreign markets easier. In addition, software can be translated upon request.

Both a research institute which develops software and a center for computer training, this firm exports some 150 types of software, primarily to the FRG, Austria, Switzerland and England. It markets several hundred in Hungary and in German-speaking countries.

One of its goals is "to expand the development of its exports of computer knowledge, especially in Iraq, Syria and Kuwait."

It offers training to its clients, i.e., to firms that buy imported computers from it. "We have 1,000 students in this category. For example, we have been training operators at Videoton for 10 years," stated Kalman Nagy, director of Szamok. This is the area which makes the most profit.

Last year the Szamok Institute implemented a program at the secondary school level (secondary schools in Hungary are equipped with several hundred microcomputers).

Szamok has the largest computer science library in Hungary, with over 70,000 references and some 300 books and scientific journals. A staff of 360 spends all its time developing software, such as Mapros, Tiptop, Printmaster, Tachomaster, Menu, Answer, Albert, Agnes, Cutplace, Dimacs, Satir, Pharmacontrol, Aromo, etc.

Szki Consulting

Founded in 1968, the Institute for the Coordination of Data Processing (abbreviated in Hungarian as Szki), is one of the largest in the area of computer research and development. Szki works on developing software products, firmware and hardware in Hungary and in all the socialist countries, as well as in Canada, the United States, Japan and Western Europe, especially in France, Sweden, Italy, England and the Benelux countries.

This institute specializes in scientific methods research, in developing hardware and system software and in developing applications software.

Its turnover, which went from 448 million forints in 1982 to 740 million forints in 1983 (about 131 million French francs) can be broken down as follows: 60 percent for applications, 13 percent for hardware, 20 percent for the export of software, 7 percent for consulting activities.

Szki software packages for individual business computers operate under CP/M and MS-DOS. The applications are numerous, including inventory management, inventory control, production control, office automation with word processing, agriculture, statistics, project management, software development, etc.

Szki has developed various types of minicomputers and functional blocks that are ordered by many national and foreign computer manufacturers.

For example, a family of microcomputers based on an LSI [large-scale integration] microprocessor is one of the most significant results of the research work of the Institute.

It consists of a complex modular set of hardware, software and programming.

Today more than 35 different systems are in service, both in Hungary and abroad.

Laszlo Binder, assistant sales manager at Szki, noted that "the first microcomputer marketed by the Institute in 1982 was the MO 8X, quickly followed by the Proper 8 and then the Proper 16 during the second half of 1983. The goal for 1984 is to develop the Proper 32."

Szki, which has a staff of 500, of which about 400 have university training, is also developing software packages for firms that intend to purchase a computer, which means that they can be ready to use data processing.

The Institute is also engaged in consulting and software development. It also adapts, develops and installs applications systems and trains user specialists.

Remote data processing is one of the Institute's goals, as is the development and application of input-output units for image and sound processing.

Also exhibiting in Grenoble, Comporgan System House, founded in 1970, is directed by Karoly Pogany. As he has stated, "The goal of this Hungarian company is to organize and apply data processing."

The Thousand Hands of Comporgan

With a staff of about 300, of whom over 200 are professionals (analysts, programmers, etc.) and who have an average age of 30, Comporgan develops different systems, especially in ICL computers, on TPA's (Hungarian) and on Commodore 64's (for gastronomy) and Commodore 710's (for the hotel business).

The basic system for these computers is the Siva system (the goddess with 1,000 hands), the national system which is number one on the Hungarian hit parade.

This system was put on the market 7 years ago as a remote processing system (in conversational mode). Two-thirds of the employees speak foreign languages, including Swedish and Japanese.

In 1983 Comporgan's turnover was $1.5 billion and its goal for 1984 is simple: to double that figure.

Karoly Pogany stated that currently "over one-quarter of the turnover comes from exports to Western Europe."

He definitely intends to increase this percentage by strengthening cooperation with Austria, the FRG, the United Kingdom, Switzerland and the United States. However, he regrest the lack of relations with France in the software field. He hopes "to find a solution with a French commercial software basis."

Comporgan is pursuing three directions for export: public health and hospital management, agriculture and applications such as telephony, networks, compilers, etc.

Some of Comporgan's clients are Diebold, Ericsson (Sweden), Hospital Computer (FRG), ICL, the British PTT, the Transportation Control in England, banks in the FRG and Austria, etc.

Videoton's Personal Computer

Videoton, which is one of Hungary's big businesses with 20,000 employees, has announced something new: a microcomputer called, for the moment, VT8/16.

IBM compatible, it operates under CP/M and CP/M+ in an 8-bit version and under MS-DOS and CP/M 86 in a 16-bit version.

Its other characteristics are a 128 kbyte main memory that can be expanded to 256 kbytes; a 5-and-1/4-inch or 8-inch (1 megabyte) floppy disk; a Winchester disk with 5 to 20 megabytes per disk; interface for a Centronics printer; and a serial RS232C interface.

Videoton is planning on making 4,000 of these models in 1984 and exporting 3,000 to Western Europe.

"Videoton is definitely oriented toward exports," emphasized Csaba Barath, sales director.

About 75 percent of total production is exported, with 15 percent going to Western Europe and the United States.

Videoton manufactures microcomputers such as the 8-bit multistation VT-30's, terminals such as the VDN 52578, character printers and line printers (under a Dataproducts license).

Videoton is the largest Hungarian manufacturer of finished electronics products. It employs 10,000 for manufacturing and 1,000 in its research institute. It has three divisions: popular electronics (32 percent), professional electronics (25 percent) and data processing, which accounts for 43 percent of the firm's turnover. These three divisions have their own development departments.

Of course, Videoton also develops software, for example the Bora system, a package of programs designed for travel agencies, especially in West Germany, where Videoton has installed several hundred terminals for reserving seats, billing tickets, etc.

The data processing age has arrived in Hungary, a market of over 10 million which is attracting Austria, the FRG, Switzerland, the United Kingdom and even the United States, and which is looking for French partners.

In 1983 Hungarian data processing exports to the West (in the area of software) amounted to about $5 million, of which $200,000 went to France, or only 4 percent.

For the same year, French exports to Hungary totaled 1.3 billion French francs and Hungarian imports to France were about the same--1.2 billion French francs.

The TAP Quadro, A Hungarian Micro

Founded in the fifties, the Central Institute for Physical Research covers several hectares. It is, in fact, made up of five independent institutes where some 2,000 people work.

The five institutes are the Measurement and Computer Science Institute, the Nuclear Energy Institute, the Research Institute for Particles and Nuclei, the Research Institute for Solid Physical Bodies and the Microelectronic Research Institute.

These institutes sometimes cooperate with each other.

For software development the Institute builds PDP8 and PDP11 compatible central processing units and buys peripherals.

At the present time over 500 turnkey systems are operating in Hungary according to Peter Forro, deputy director for science at the Central Institute for Physical Research. The Institute sells its systems in the socialist countries and also in Algeria, Finland and the United States.

About 120 systems are developed each year for each computer model. The product exhibited in Grenoble is the TAP Quadro, a micro version of the TAP 8 (compatible with the PDP 8).

The major development trends are measurement techniques (industrial applications and laboratory applications) and automating management (financial systems, production management systems, etc.).

Exporting

Sci-L, a subsidiary of Szki directed by Gyozo Kovacs, was founded in January 1982 and has a staff of 75.

Its primary purpose is to be involved in activities abroad. Its functions are to export business computers with after-sales service.

Szki has a sizable software library, an advantage when exporting. For example, there is the Prop-Optimix program designed for agriculture, the Prop-S-Text word processing system; Prop-Microbomp, a software package for preparing the production and management of technical source data; Prop-SCS-2000, a system for warehouse management and administration. Remember that in 1982 Szki opened M-Prolog, the school for logical programming in Hungary.

Szki's goal is to find new markets and new clients to add to its existing list of Siemens, Diebold, Software Engineering Service, Bull, Ericsson, SMT Goupil, etc.

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LABORATORY ANIMALS FOR PHARMACEUTICAL RESEARCH

Budapest MAGYAR HIRLAP in Hungarian 14 Apr 84 p 13

[Interview with Ferenc Hargitai, vice president of the Hungarian Association of the Pharmaceutical Industry, by Istvan Palugyai, reporter: "The Victims of Science"]

[Excerpts] Animal Factories

The Hungarian pharmaceutical industry has somewhat lagged behind in developing the research base for biological studies and it is now trying to remedy the losses with the support of the National Committee on Technical Development. Ferenc Hargitai, vice president of the Hungarian Association of the Pharmaceutical Industry, puts it in these words:

[Answer] The biological studies preceding the clinical tests cannot be neglected--both from the standpoint of competitiveness and, moreover, of keeping alive on the international market. And it is a strict rule in pharmaceutical research that the effects of the compounds examined must be studied on several animal species.

[Question] Where are the experimental animals raised in our country and how great is the demand?

[Answer] First of all, I should mention a few numbers. In 1983 in Hungary, 561,000 mice, 191,000 rats and 9,000 guinea pigs were sacrificed on the altar of science. Sixty percent of these were used by pharmaceutical research establishments.

A total of 12,000 came from SPF [Specific Pathogen Free] strains although, after completion of the current expansion, we should like to boost this number of 250,000. The largest "animal factory" is the Laboratory-Strain Animal Breeding Institute (LATI) in Godollo; in addition to institutes of the pharmaceutical industry, it also supplies the academic and health research networks. However, LATI is unable to satisfy the demands in every respect in spite of its enormous capacity. In the development program, we plan the construction of a new section by the end of the Sixth Five-Year Plan period through which the institute would serve for a long time as an adequate base of laboratory animal supply for biological research.

Expensive Beagle

[Question] What do they raise in Godollo?

[Answer] In addition to the rodents also cats this year. The breeding stock is bought from West Europe and, after completing the reconstruction, 4,000 animals will be placed at the disposal of the scientists each year. Another great undertaking within the program is the dog kennel under the guidance of the Institute of Pharmaceutical Research, Joint Enterprise. They raise the so-called beagle species, found best suited for research. The enzyme system of these long-eared, flat-furred, unusual dogs the size of spaniels shows the greatest similarity to the human system; therefore, studies using them are accepted the world over. They are very valuable creatures costing more than $1,000 apiece. The breeding stock animals are even more expensive. Four years ago we bought 40 of them and started breeding them in 8 large stables. This year, about 600 such dogs will be delivered from the kennel and next year possibly 700. The expensive dogs can also be exported, which is not bad business, indeed.

[Question] Other animals?

[Answer] Starting next year, domestic research will also need about 150 dwarf swine. These, however, are less costly to import because of lower demand. On the other hand, preparations are being made for a cooperative venture between LATI and owners of the monkey colony in Suhum. In some experiments, monkeys are nearly irreplaceable. Nevertheless, work with them is represented merely by trials with 5-6 rhesus monkeys and chimpanzees. According to the plan, we should start the domestic breeding of monkeys by adapting Soviet methods.

Humane Aspects

[Question] What role is assumed by the individual domestic pharmaceutical houses in the program supported by both the OMFB [National Committee on Technical Development] and the Ministry of Industry?

[Answer] It is not worth while to breed laboratory animals at too many places. However, the conditions for their upkeep and for research using them must also be provided at the individual enterprises. The expansion of biological research capacities--which also means advances in instrumentation--has begun at the Pharmaceutical Works of Kobanya. The laboratory building constructed there is now being followed by one at Chinoin--unfortunately, its construction was at a standstill for years. At the Pharmaceutical Branch of the EGYT [United Pharmaceutical and Nutriment Factory] in Budapest, development will be started during the second half of the 1980's while BIOGAL and Alkaloida can rely on the Institute of Pharmaceutical Research and on the departments of the universities in Debrecen.

The complete, preclinical documentation of a new drug, in accordance with the international standard, could be done most assuredly by the GYKI [Pharmaceutical Research Institute] and, nearly at the same level, by the Pharmaceutical Works of Kobanya. The others are forced to submit certain tests to domestic, or often to foreign research institutes--in the interest of obtaining more reliable references.

The development program discussed most certainly evokes dissatisfaction in many people. I am referring to the reservations of those who protect animals, and also to the humane aspects. However, the scientists also expect the objections. The guidelines by the World Association of Pharmaceutical Industries also call attention to the requirement that the animals should suffer as little as possible during treatments. There are definite results in this respect. Namely, there had been drug experiments earlier in which half of the animals succumbed as a necessity. More recently, even such types of experiments require much fewer sacrifices. But a certain number of mice, rats and rabbits will continue to be necessary for determining the clinical therapeutic index. And even the loudest arguments by the animal lovers become dwarfed if the sensible sacrifice of animals for scientific purposes is helping millions of human lives.

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